

May 5-9, 2025

LHCP TAIPEI
2025

13th Edition of the Large Hadron Collider Physics Conference

ATLAS Upgrades



**University
of Victoria**



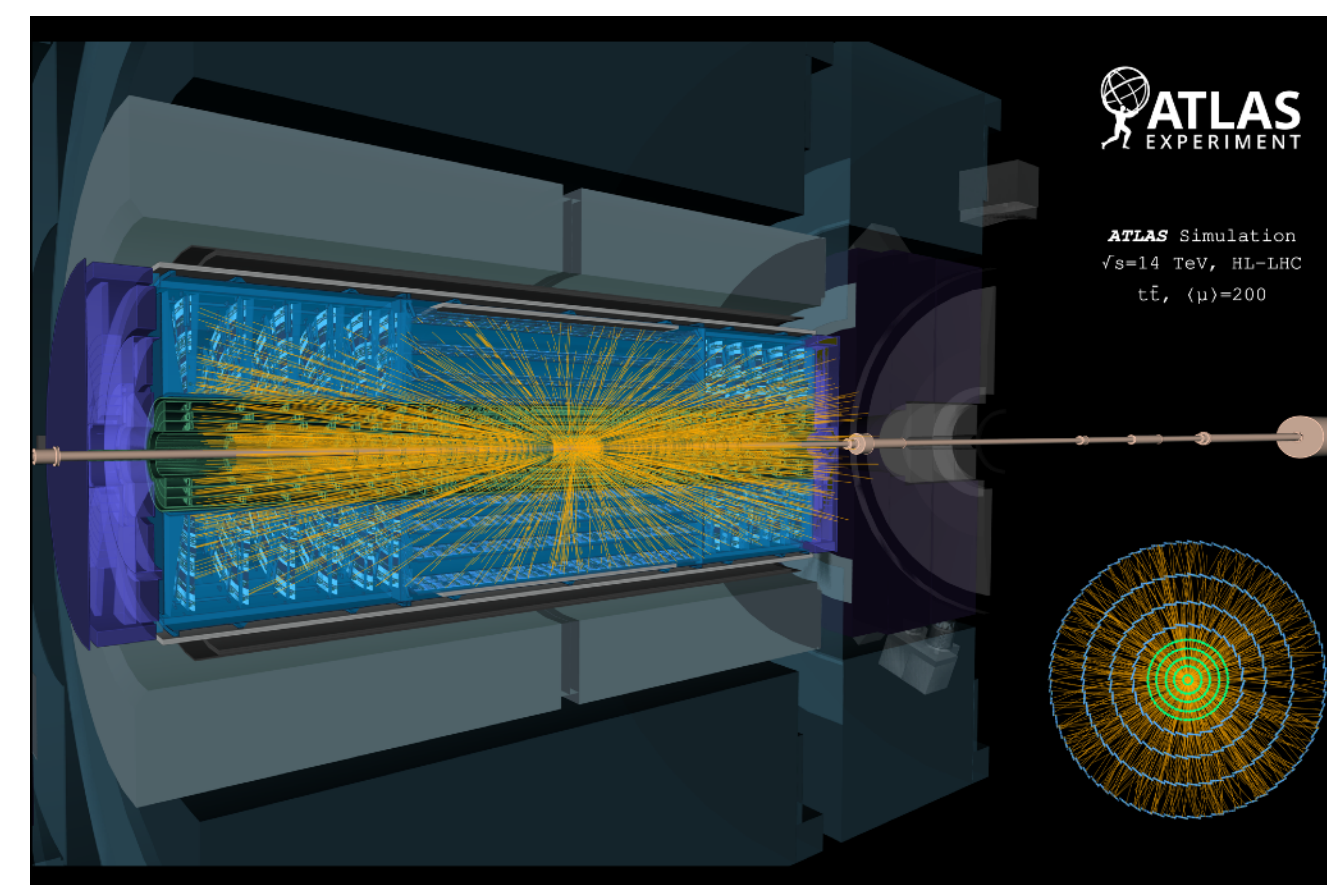
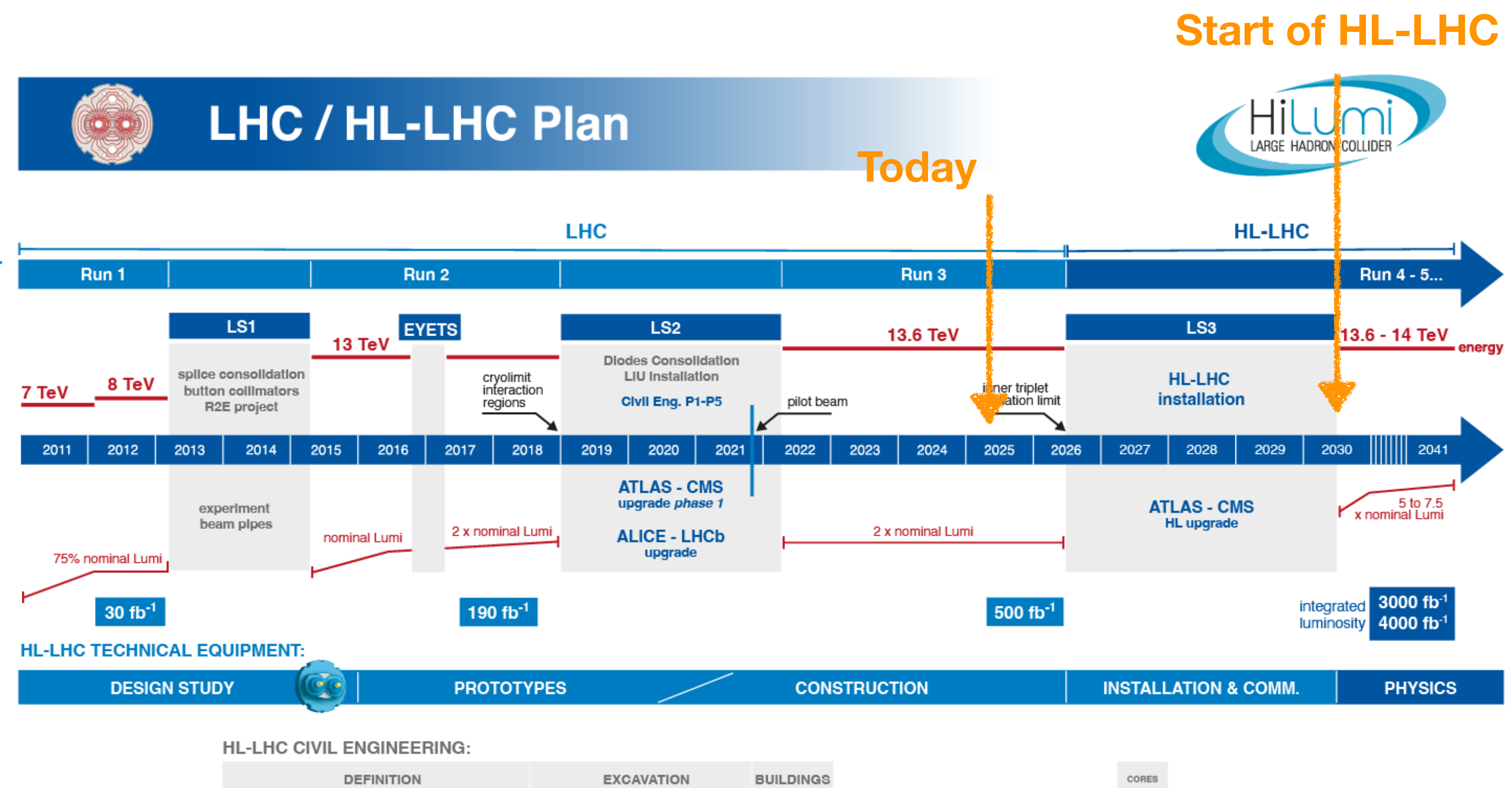
ATLAS
EXPERIMENT



HL-LHC

- HL-LHC program will start in 2030 and continue until 2041
- Aim at an instantaneous luminosity of up to $7.5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$
- Pileup will increase to up to 200 proton-proton interactions per bunch crossing
- Integrated luminosity target is 4000 fb^{-1}
- Will allow to probe the Standard Model even further and especially rare processes

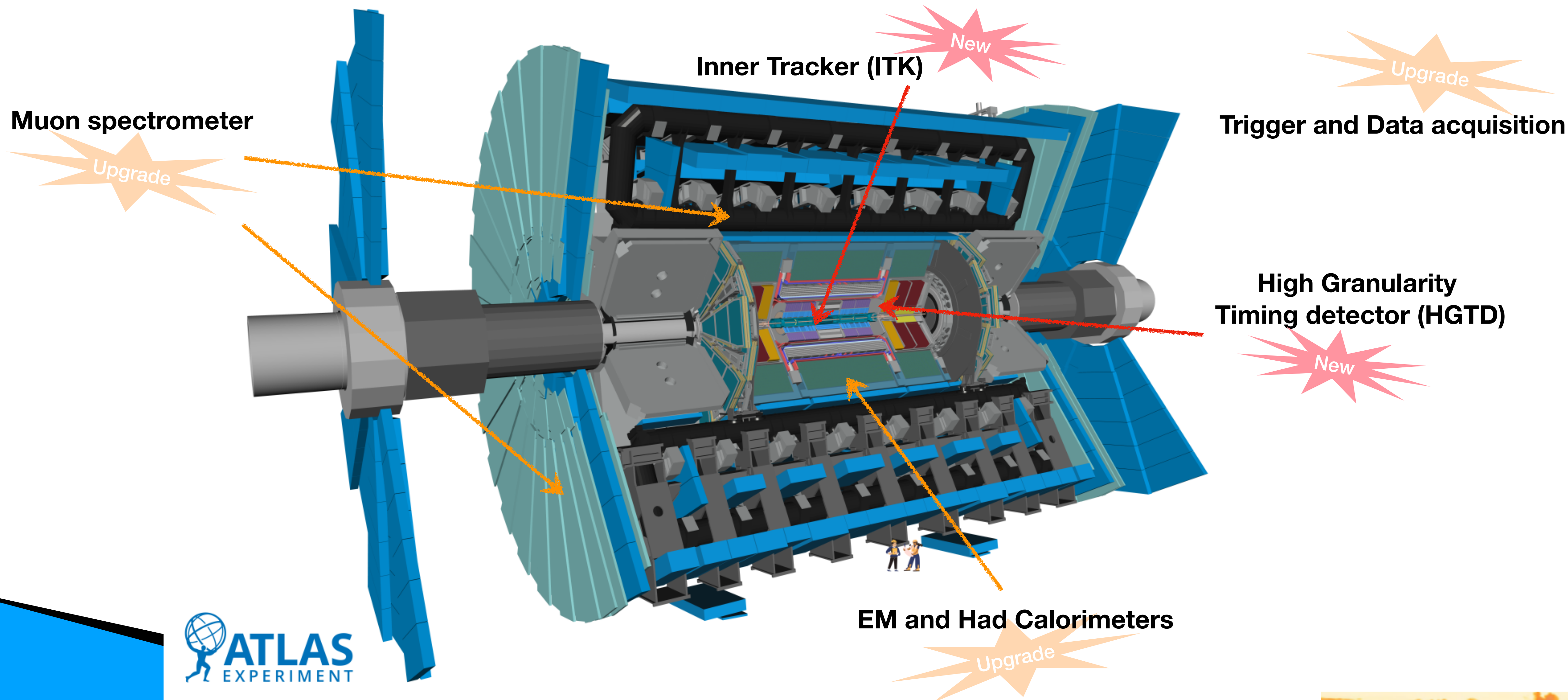
More about physics prospects in [Giordon's talk](#)



Simulation of $t\bar{t}$ event in ATLAS tracker with 200 pileup collisions

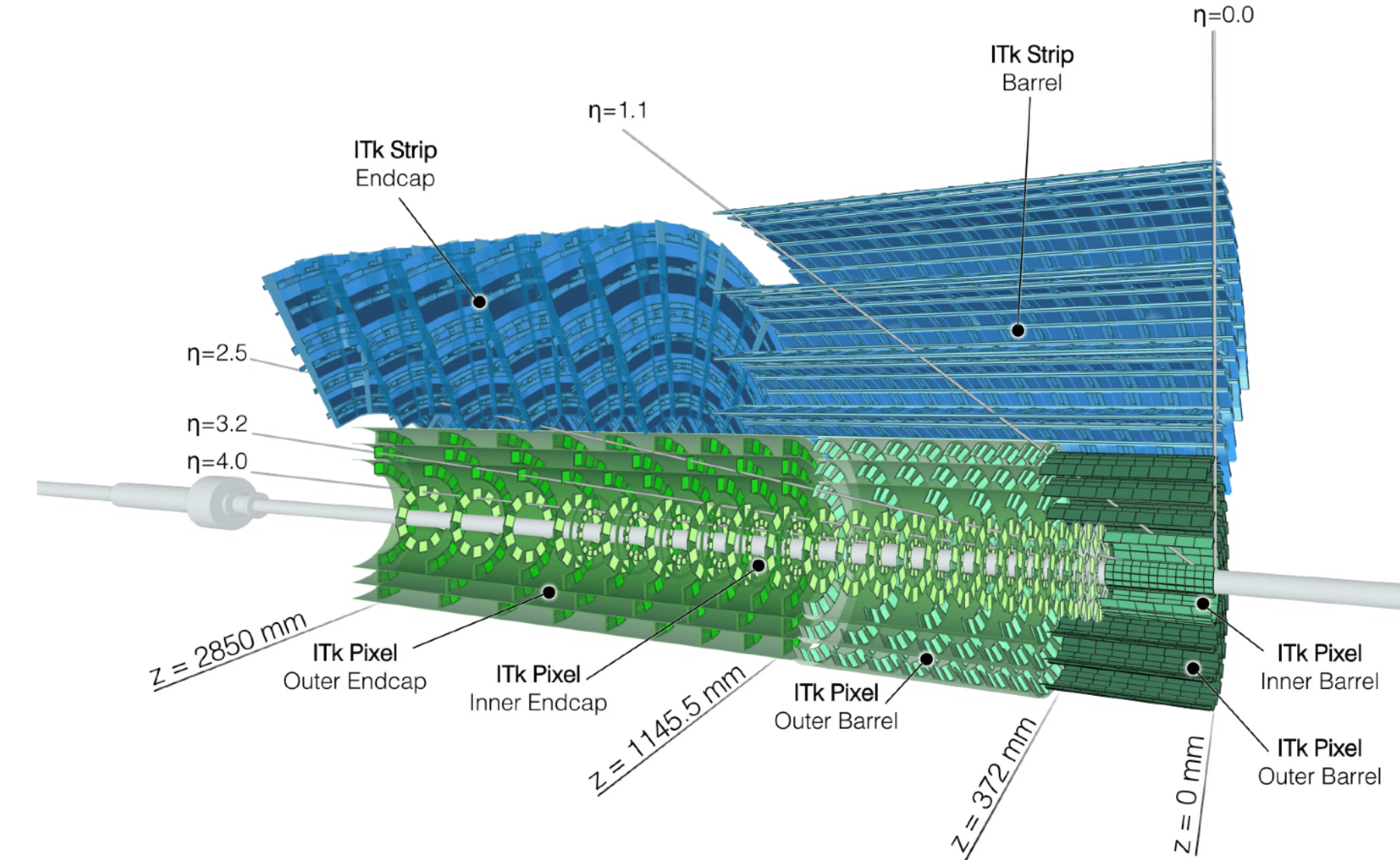
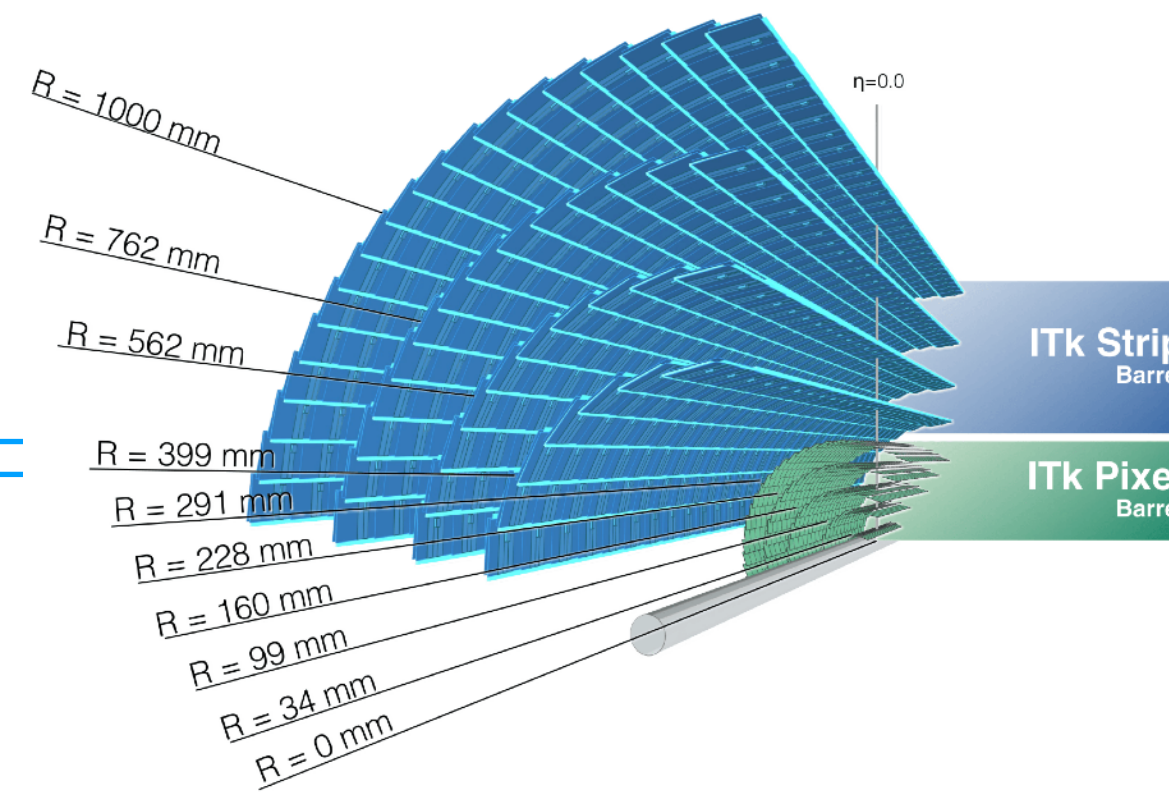
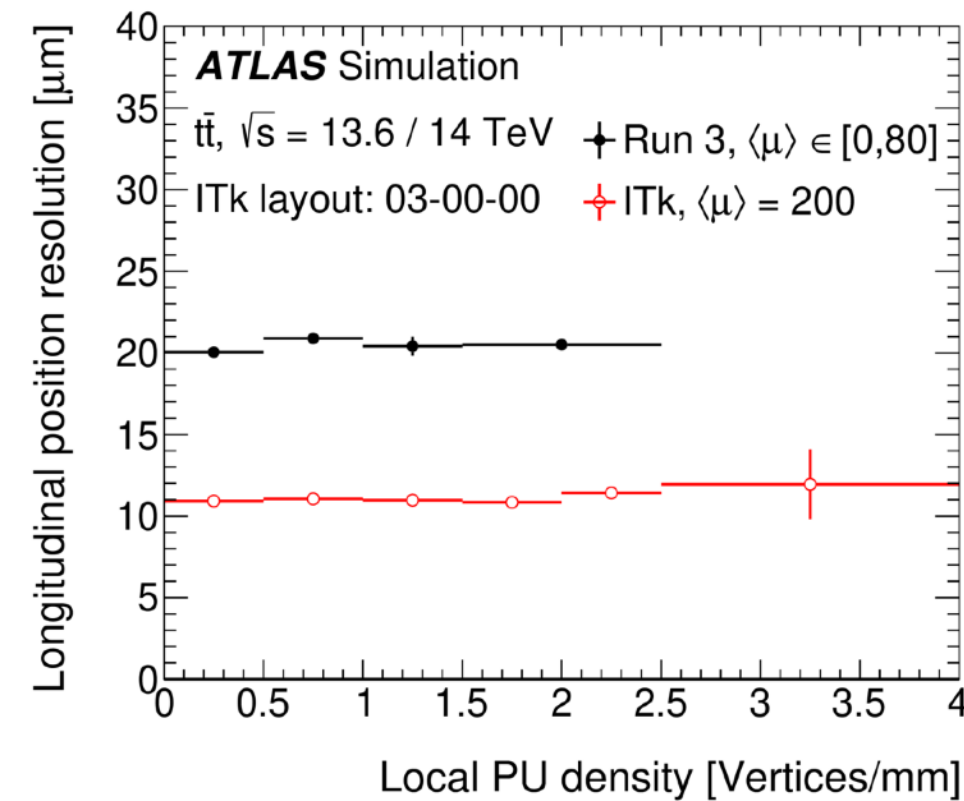
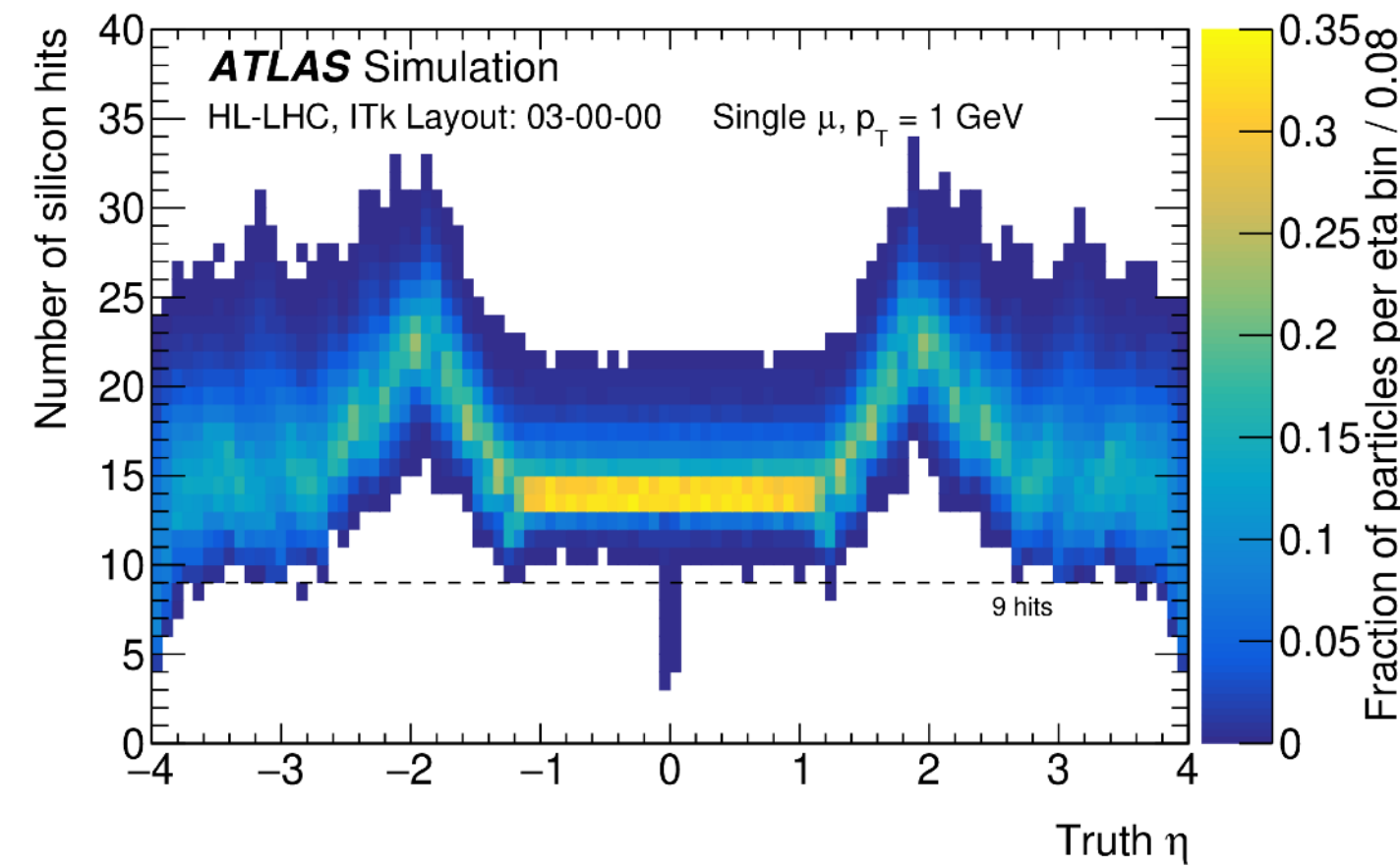
All of this require to upgrade the ATLAS detector

Overview of ATLAS Upgrade



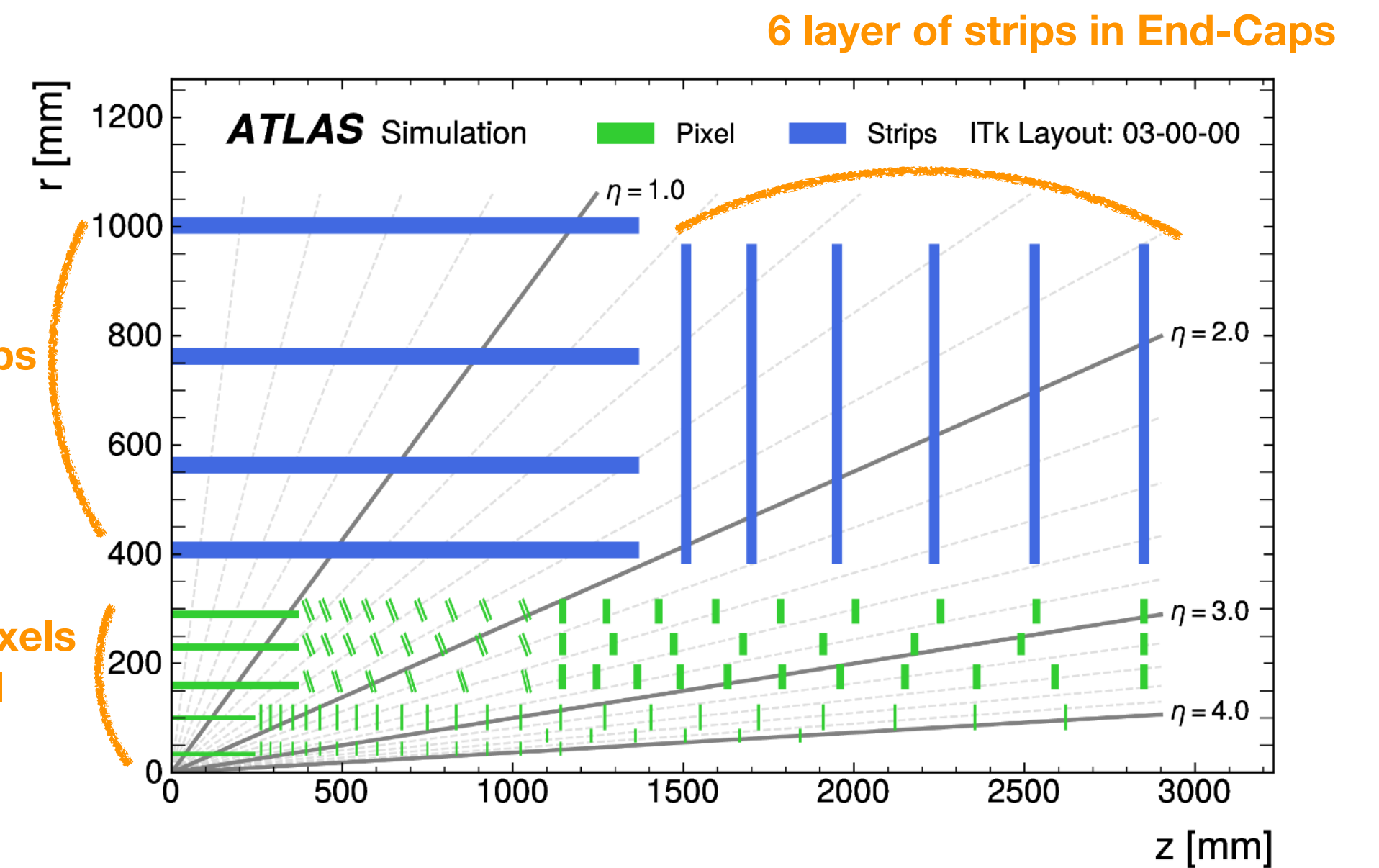
ITK

- New Tracker fully silicon based
- Pixel detectors (inner part)
 - 5 billion channels
 - 5 layers of pixels in Barrel
 - Many disks in End-Cap
- Strip detectors (outer part)
 - 60 million channels
 - 4 layers of strips in Barrel
 - 6 layers of strips in End-Cap
- Coverage up to $|\eta| = 4$
- At least 9 hits per track in the central region
- Limited material budget in the forward regions
- Robust performances at high pileup



5 layer of strips in Barrel

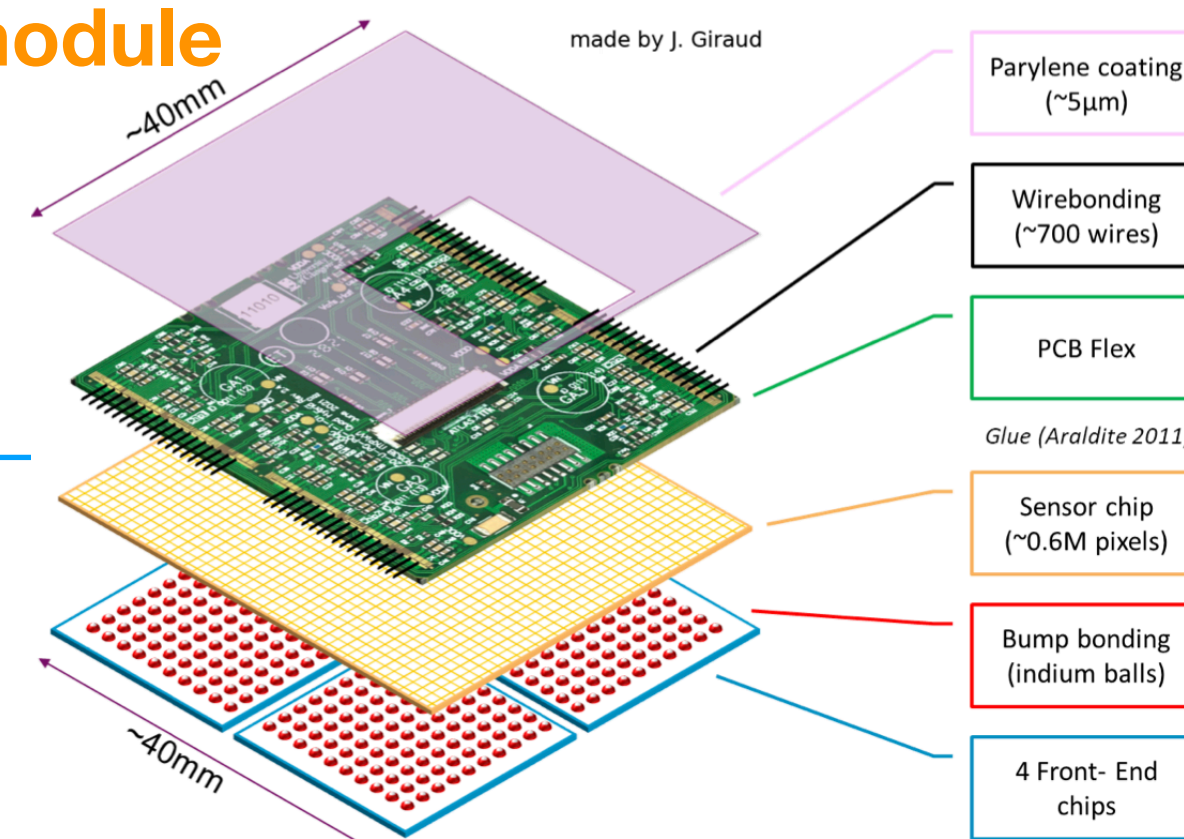
5 layer of pixels in Barrel



More details in [Hideyuki's Talk](#)

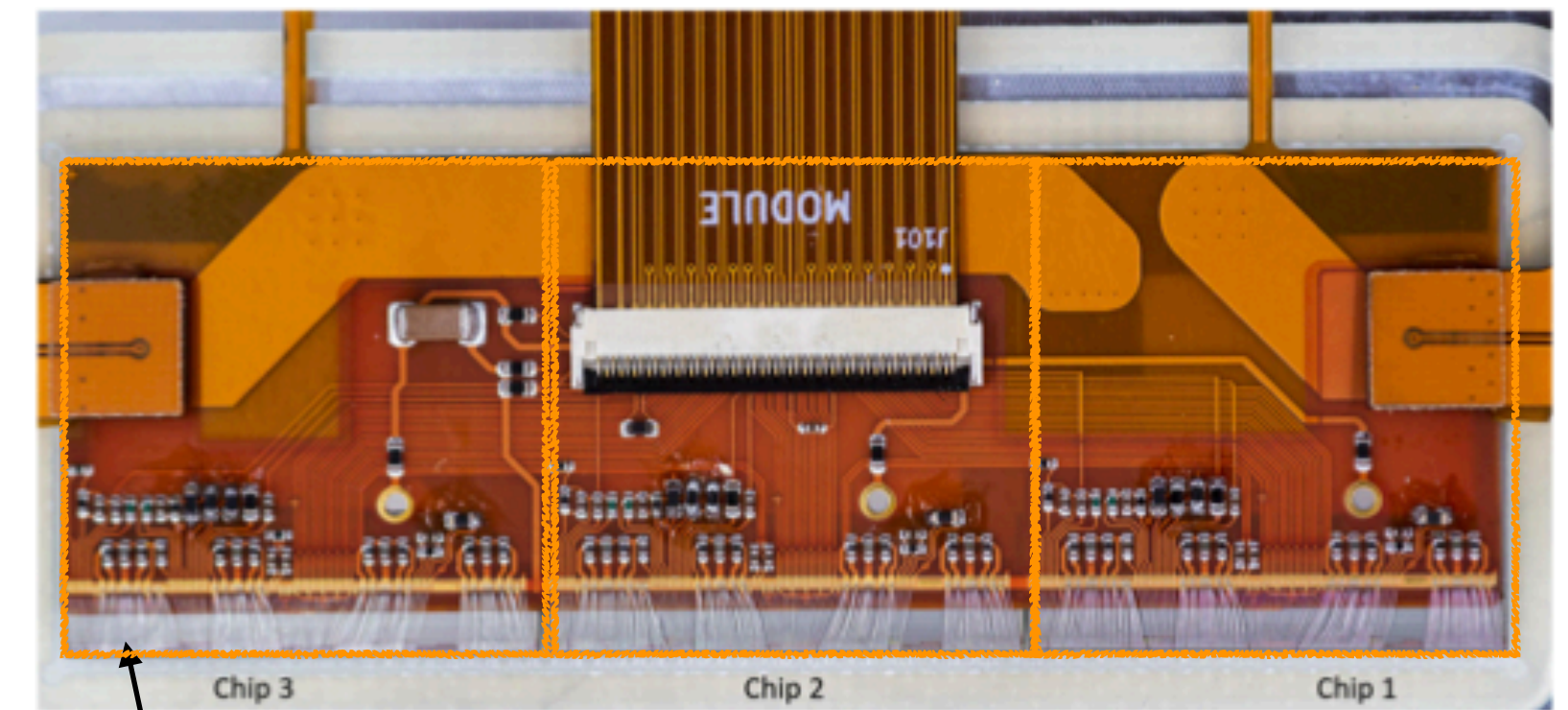
ITK Pixel

Structure of a module

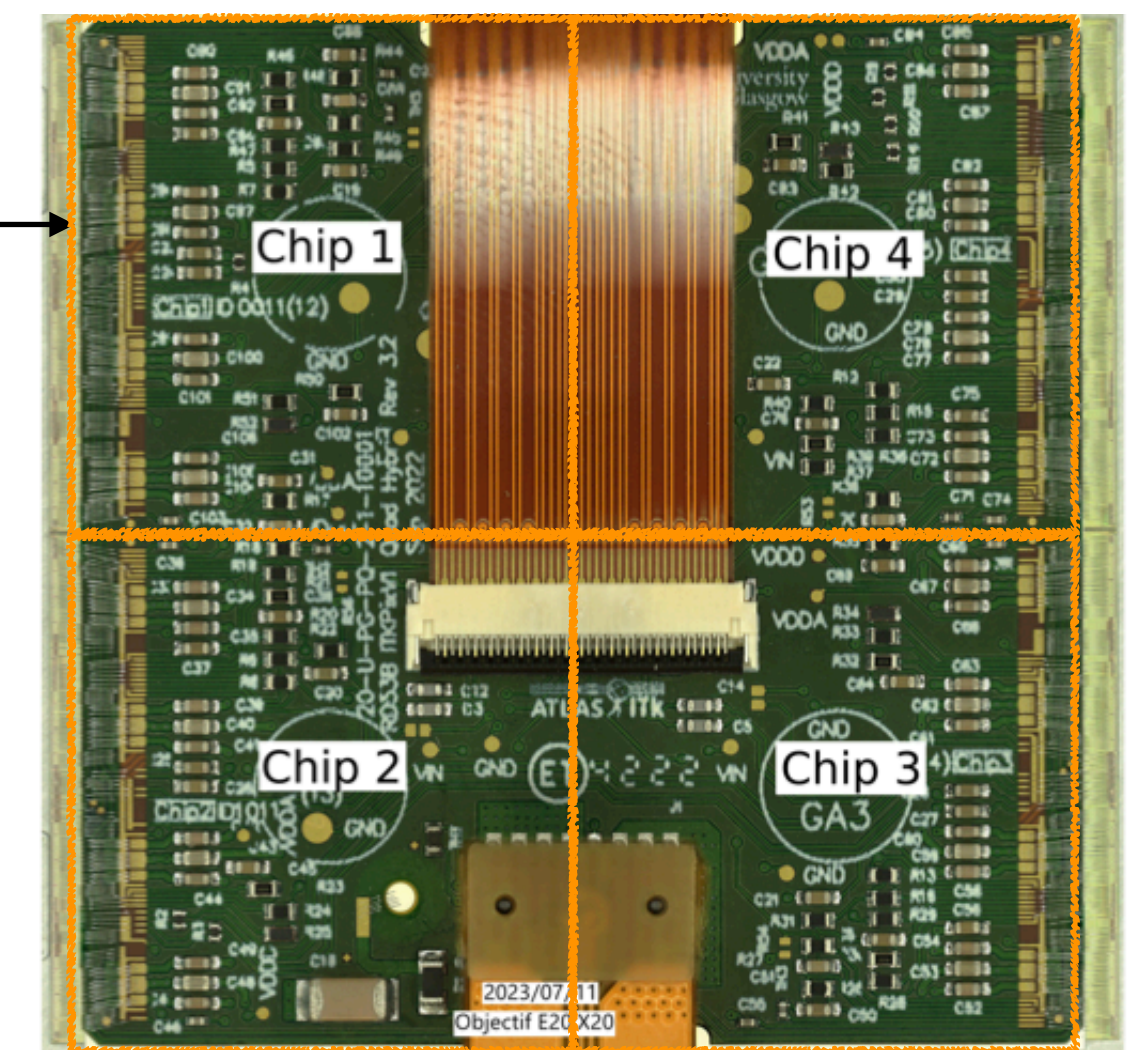


- Innermost layer of pixel uses :
 - 3D sensors technology $20 \times 20 \text{ mm}^2$
⇒ More radiation tolerant / more expensive
 - 2600 modules are needed organised in triplet (3 Front-End Chips/module)
- Other layers of pixels uses
 - n-in-p planar sensor $40 \times 40 \text{ mm}^2$
 - 7166 modules needed and organised in quad (4 Front-End Chips/module)
- In modules the sensor is sandwiched between Flex PCB and Front-End chips
⇒ Chip is bump bounded to the sensor
⇒ Flex PCB wire bonded to the Front-End chips
- Module assembly is very complex and shared over 20 institutes
- Half of production done for sensors and chips
- Started production phase for modules assembly
- Module loading on structure has started

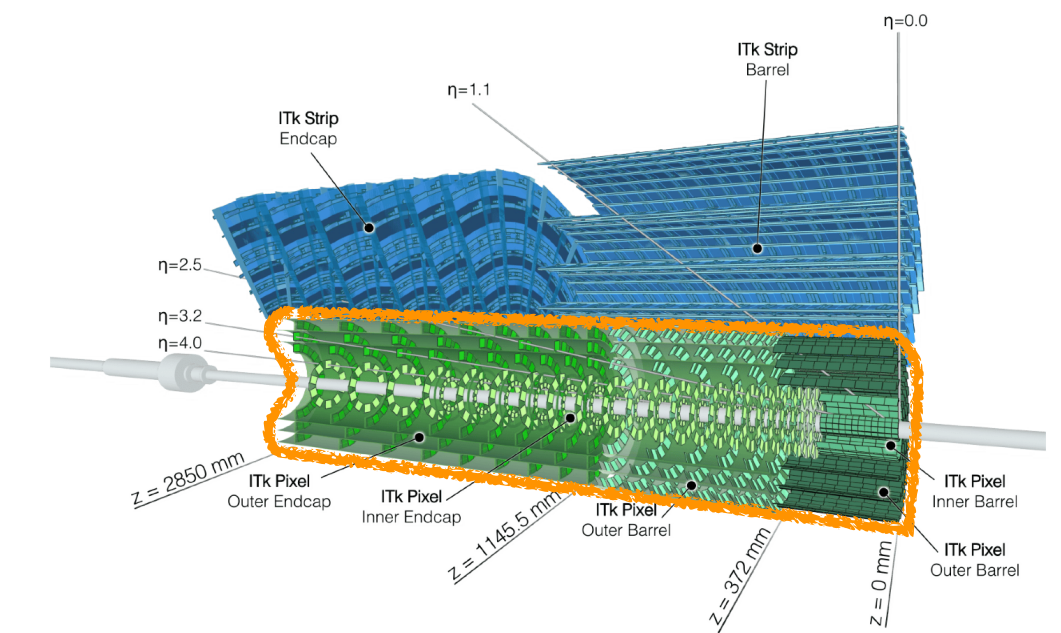
Triplet module



Wire bonds

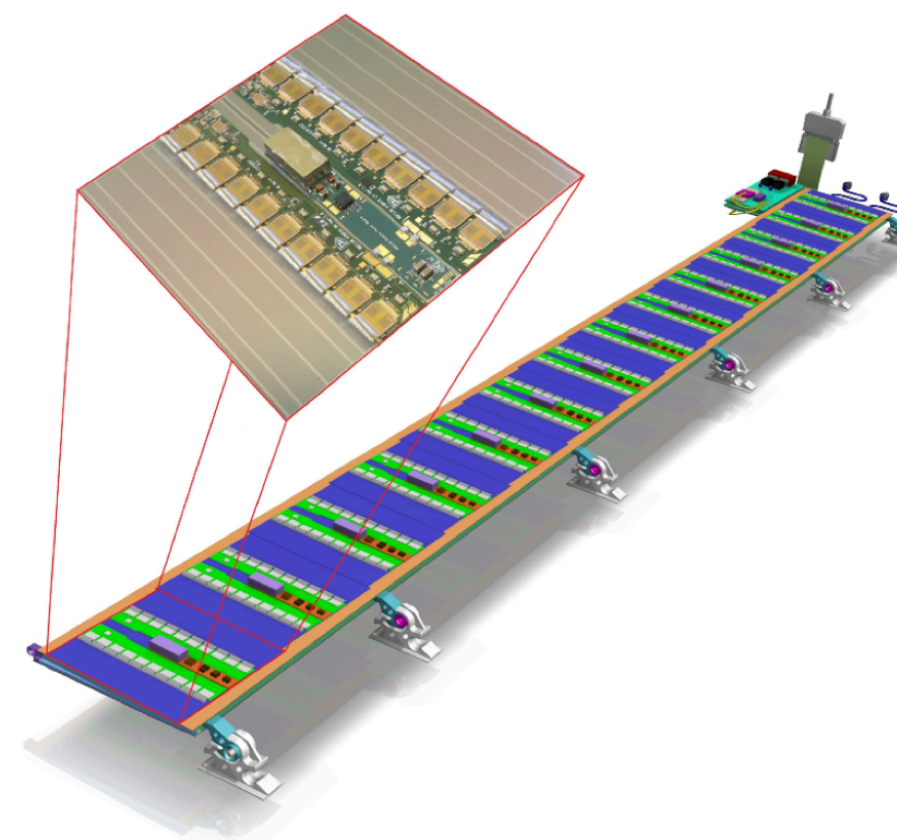


Quad module

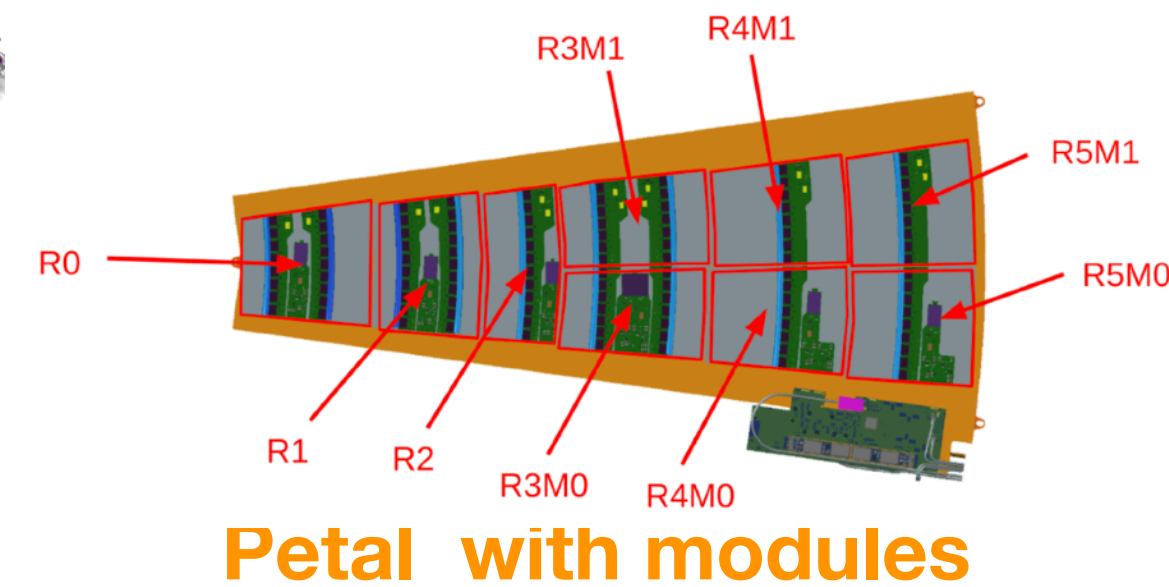


ITK strips

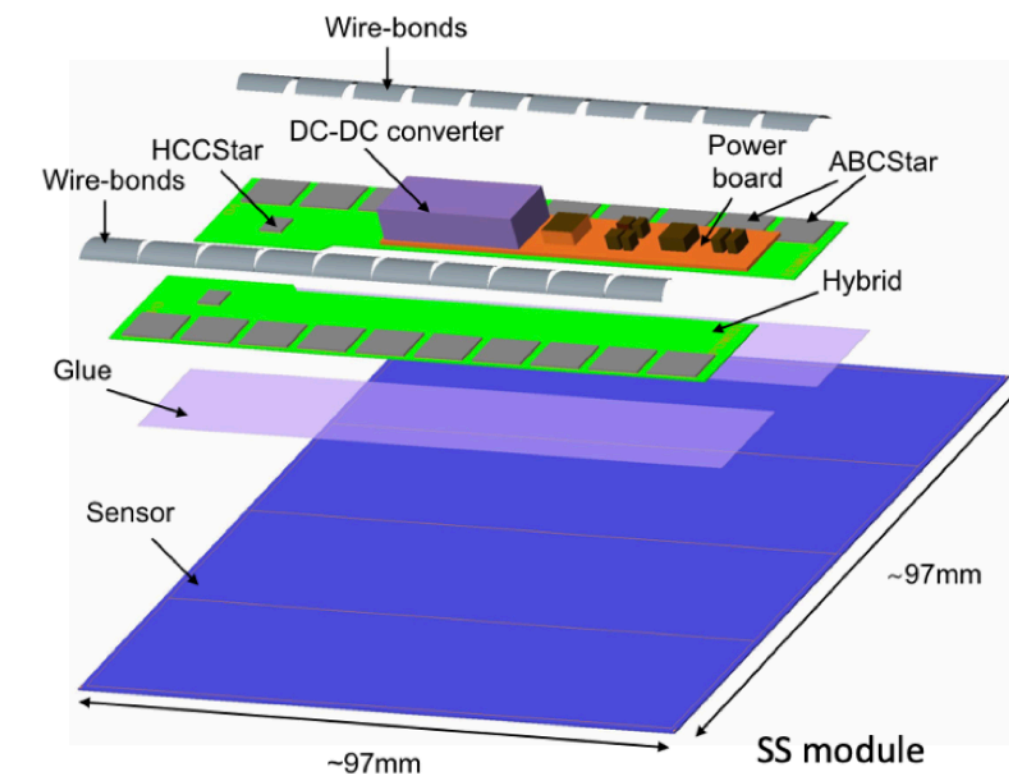
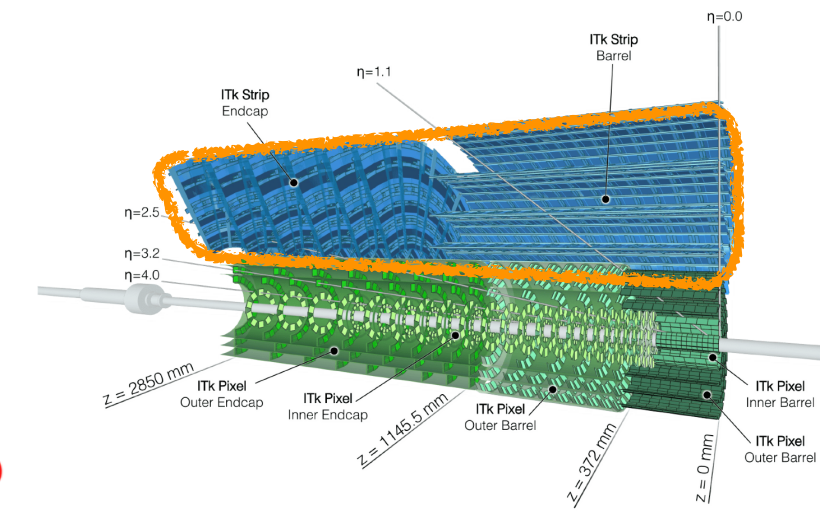
- Modules are mounted on staves for barrel or petals for end-caps
- Strip sensor has a typical size $97 \times 97 \text{ mm}^2$
- Strip pitch is $75.5 \text{ } \mu\text{m}$
- Structure of modules are
 - Hybrids hosting readout (ABCStar) ASICs + power modules are glued into the sensor
 - Strips are wire-bonded to the ABCStar chips
- 2 (6) different types of sensor for the barrel (end-caps)
- Production of sensors and ASICs close to be complete
- Production of modules assembly just started



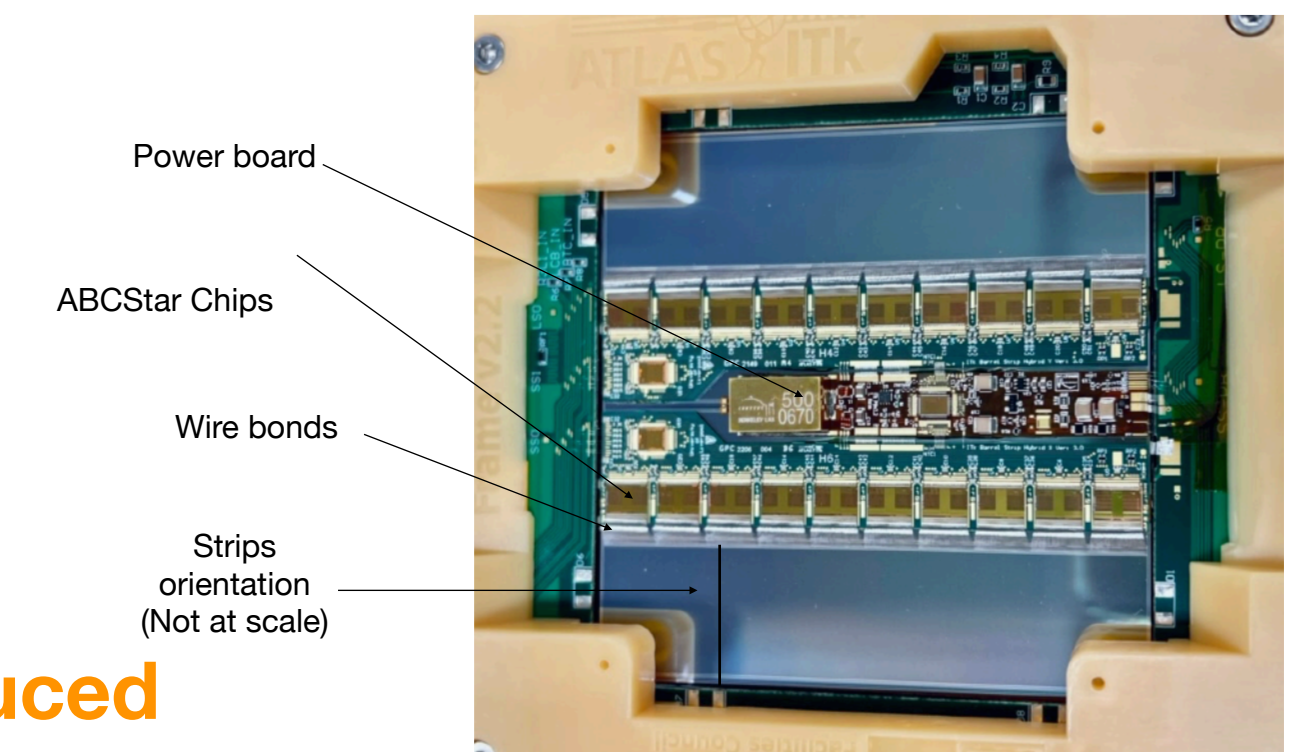
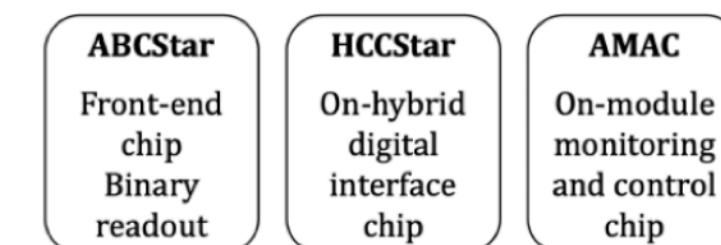
Stave with modules



Petal with modules



Structure of module

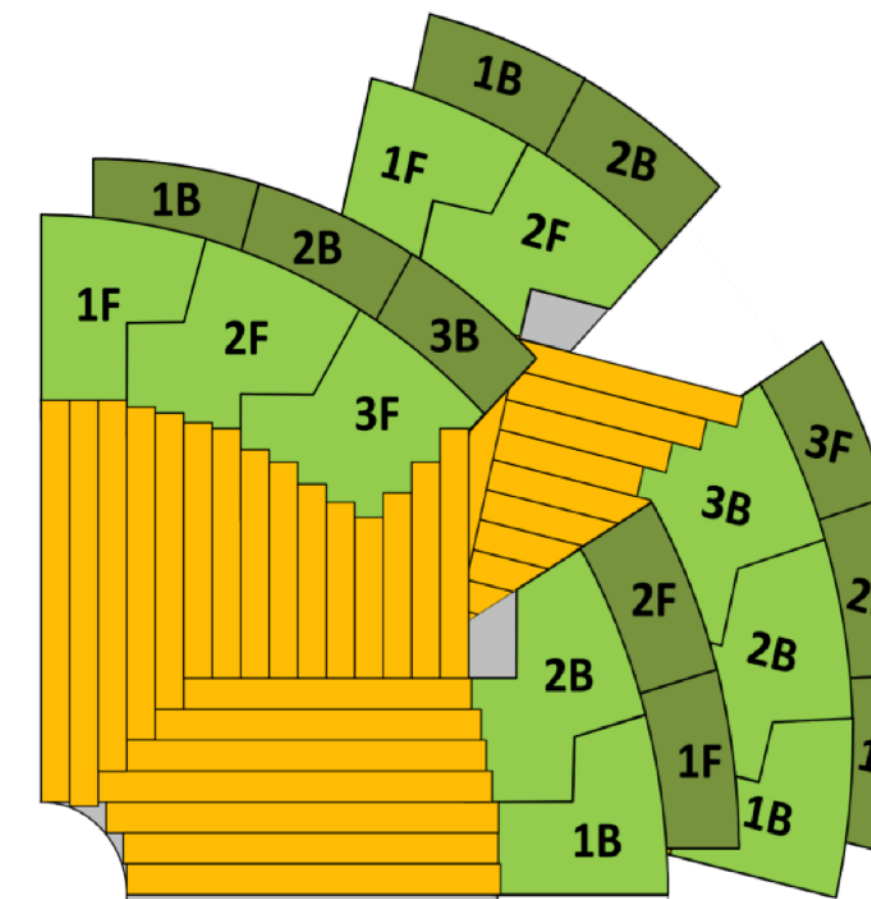
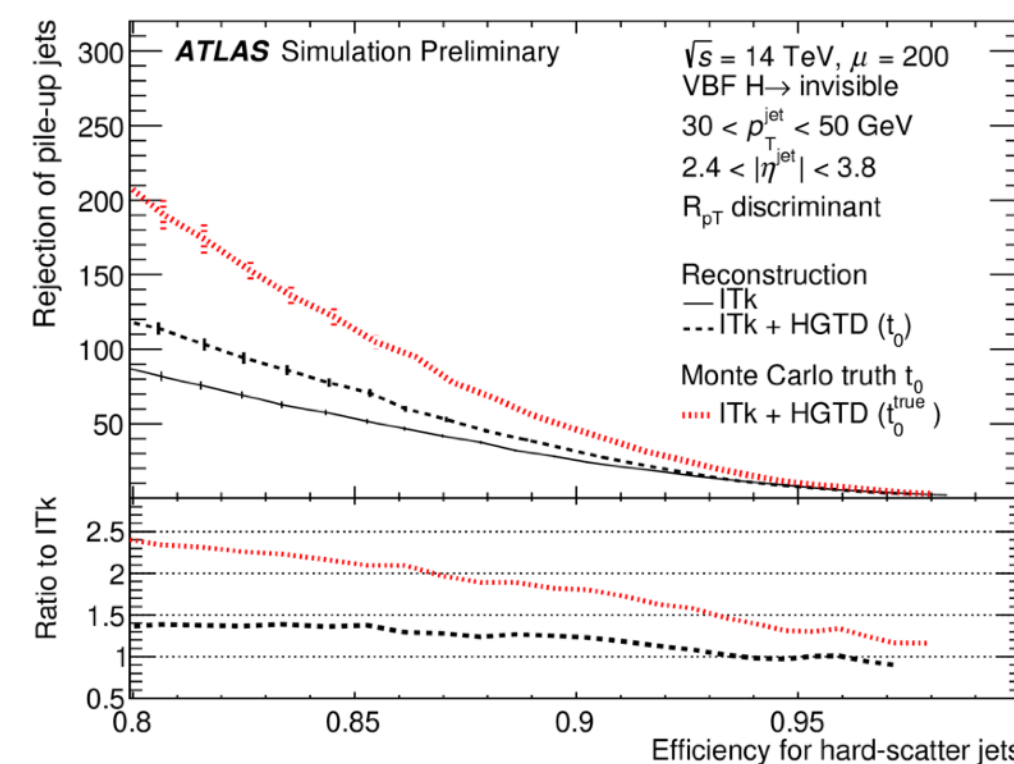
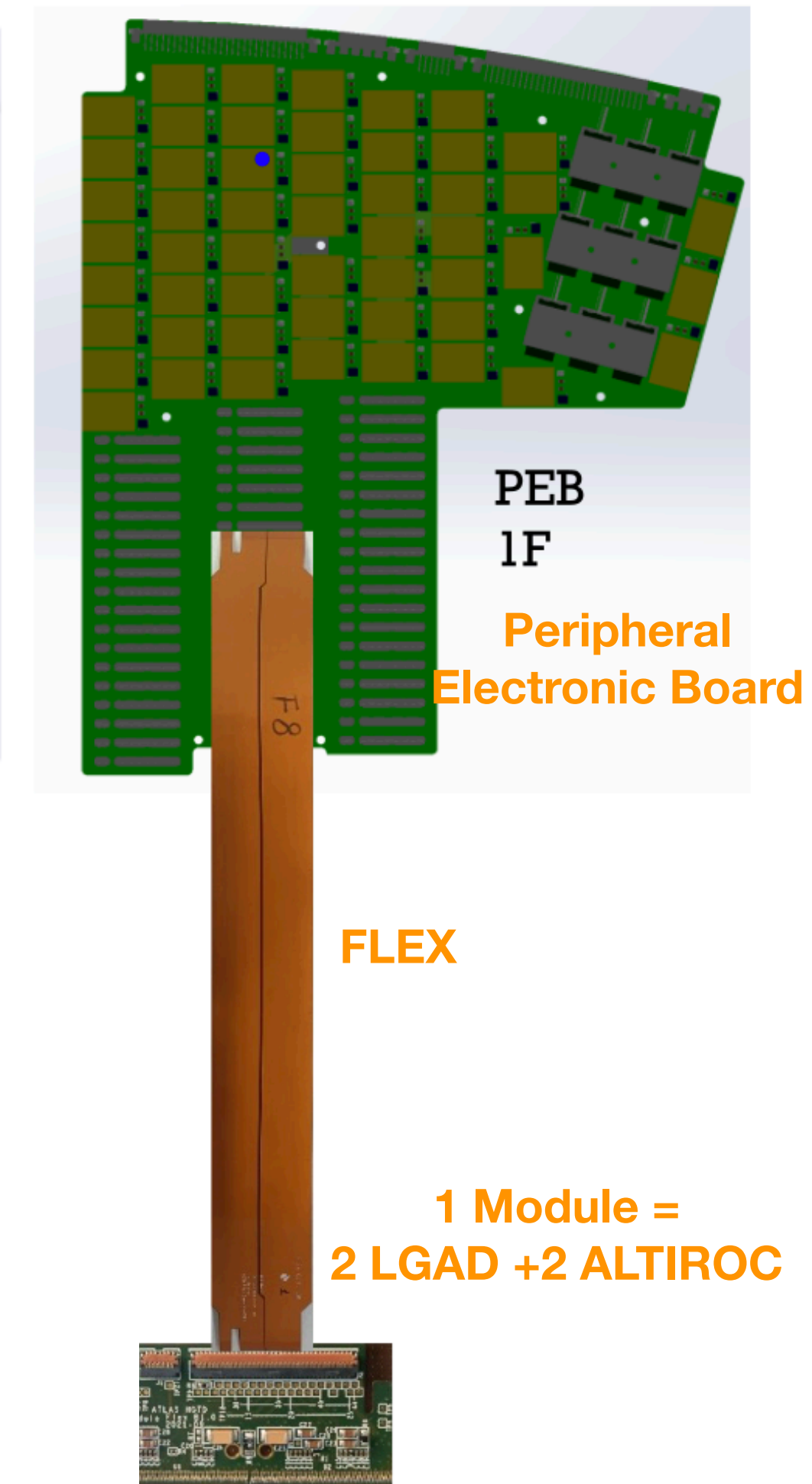
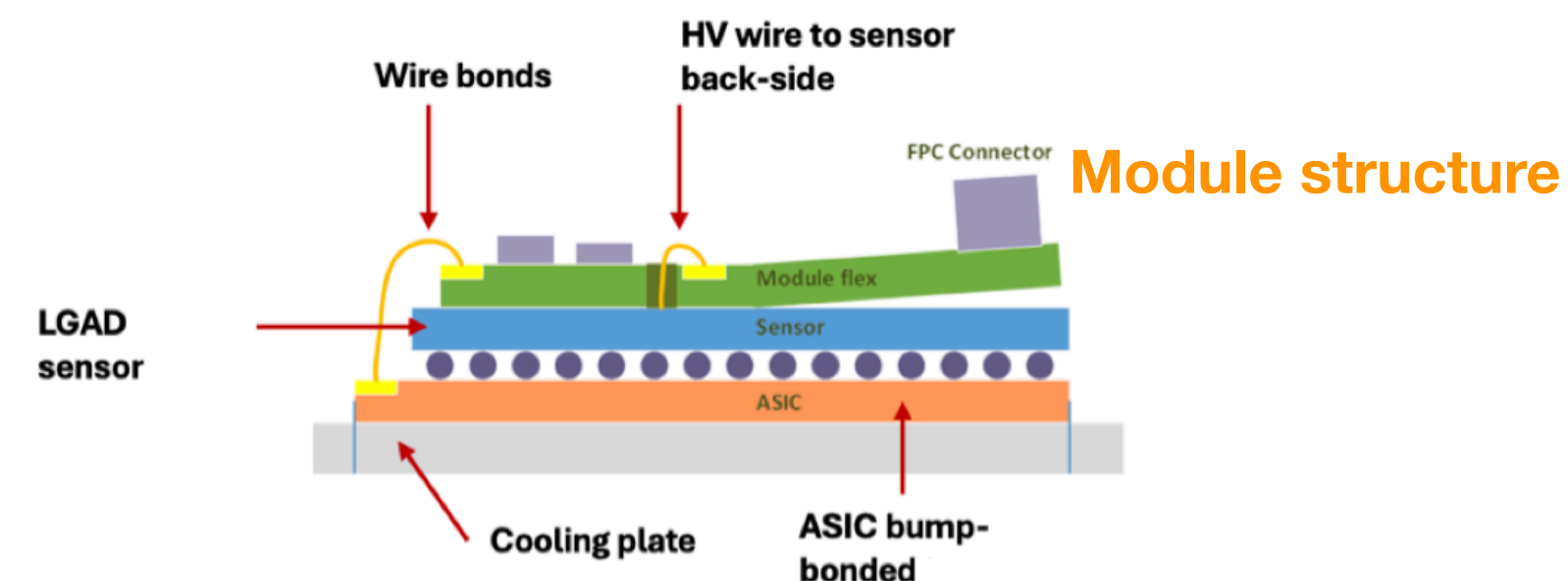
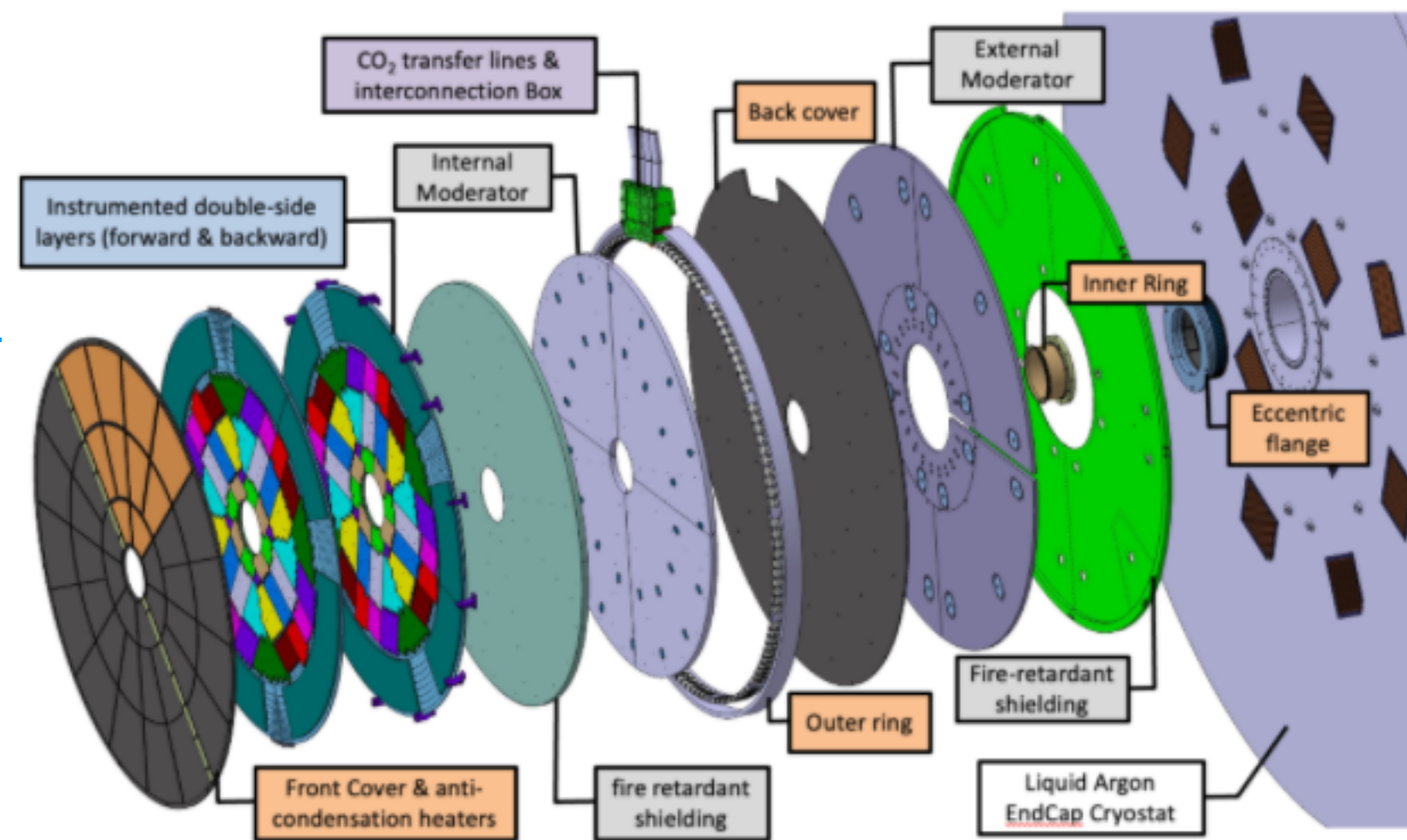


Example of produced

HGTD

- New silicon based timing detector
- Positioned between ITK and the End-Caps calorimeter
- Should provide timing resolution of 30 – 50 ps for tracks with $2.4 < |\eta| < 4$ and $12 \text{ cm} < r < 64 \text{ cm}$ allowing better pileup rejections
- Should also provide bunch by bunch luminosity measurement down to 1% uncertainty
- Two double-sided disks with 8032 modules
- Each module : 2x Low Gain Avalanche Detector LGADs bump bonded into ASIC (ALTIROC)
Production of Sensor started
ALTIROC production to start in June
- Connected via FLEX cables to Peripheral Electronics Boa that contain DC/DC converters, IpGBT chips, VTRx
Final Design Review in May

Overall structure of HGTD



Layout of PEB (green)
And readout rows (yellow)

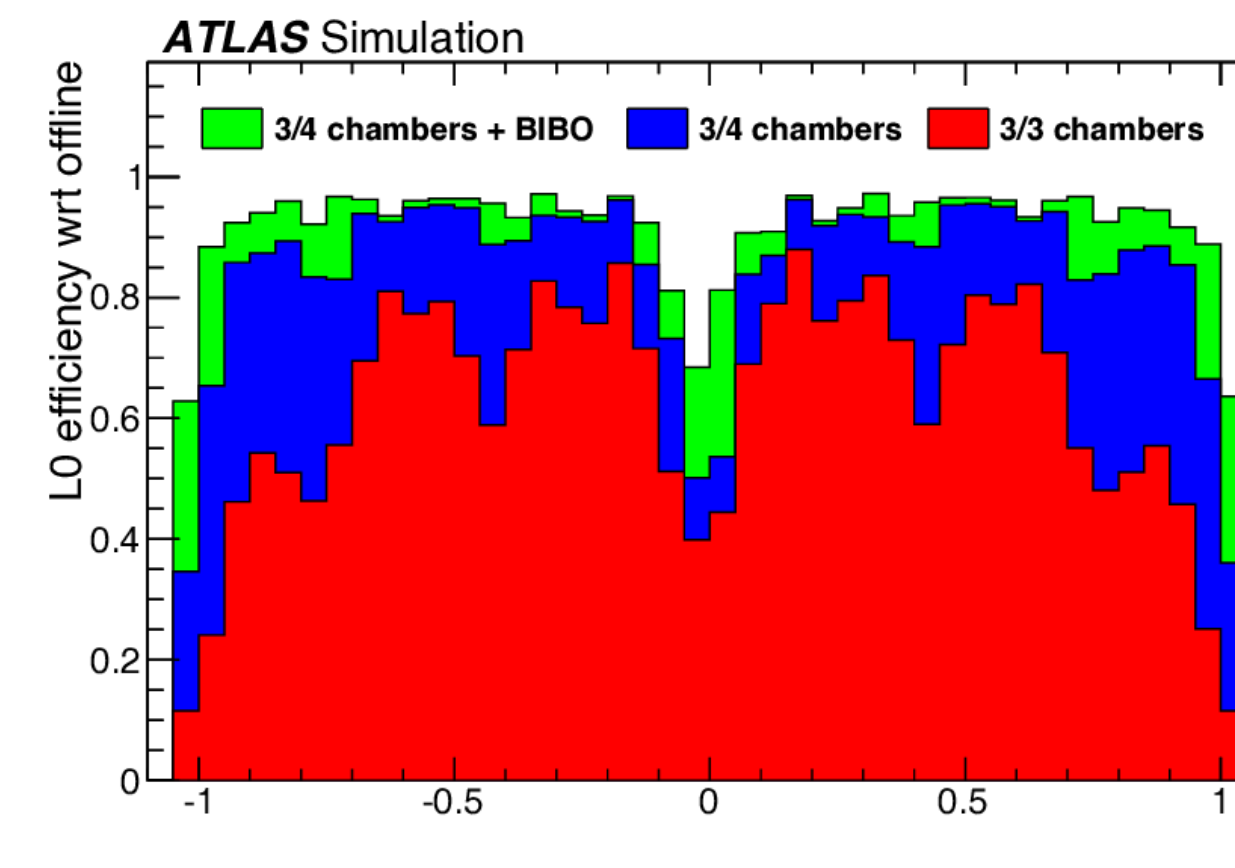
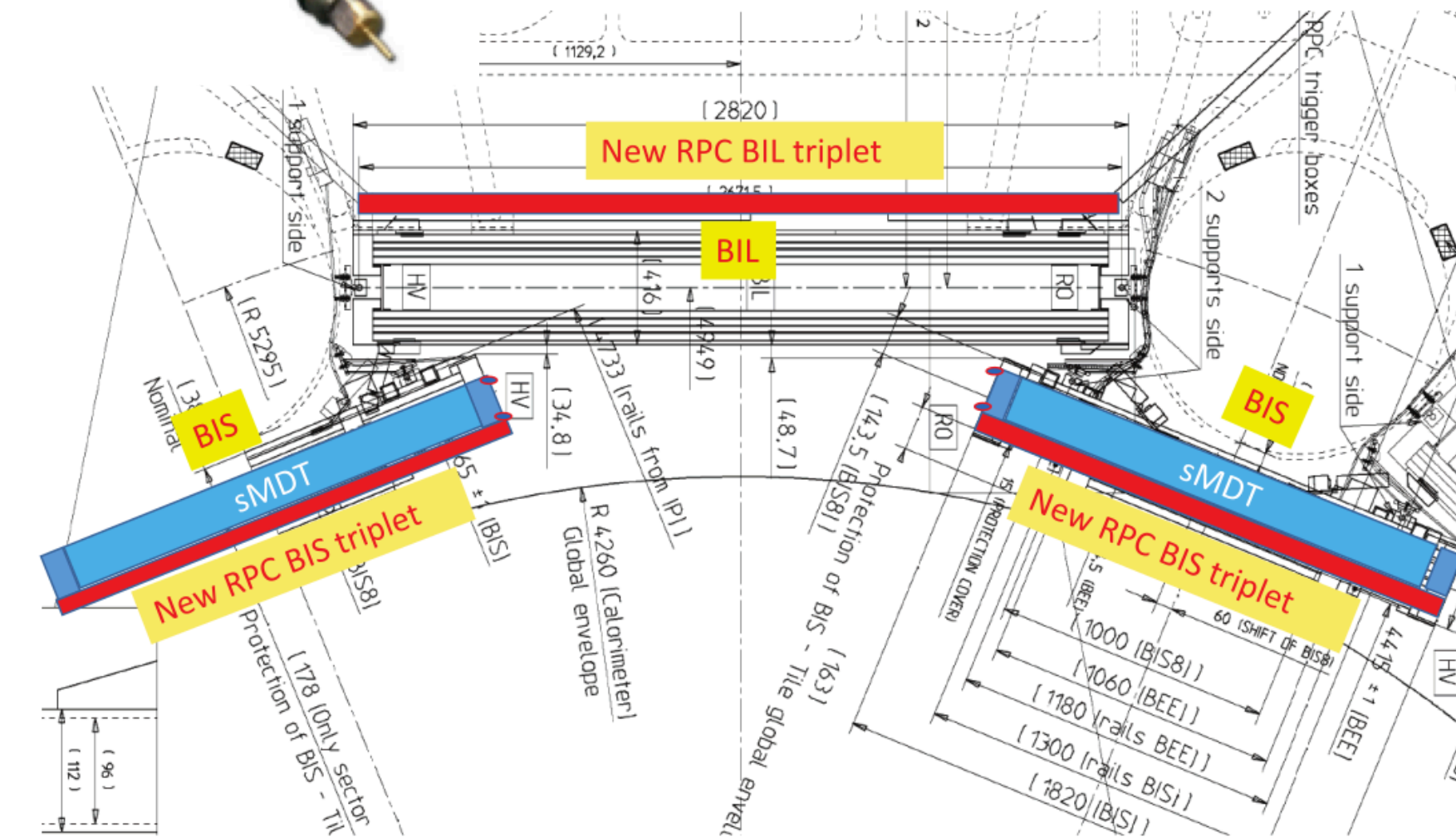
Muons system

MDT

Comparison of MDT with sMDT

sMDT

- Multiple projects with common purpose to improve trigger efficiency :
 ⇒ Increased coverage for Barrel
 ⇒ Send all data at 40 MHz off detector to perform trigger logic on FPGA
- In the Barrel
 - Small Monitored Drift Tubes (sMDT) will replace MTD in small sector
 ⇒ Gain of space allow to insert additional Resistive Plate Chambers (RPC)
Chambers are produced, integration is ongoing
 - Add RPC triplet on long sectors
- In the End Cap:
 - New Small Wheel as part of Phase-1 upgrade
 - Replace End-Cap Inner Layer 4 from doublet to triplet of TGC (same envelop)
Production ongoing / Pilot installed during last YETS
- Most of the readout electronics will be exchanged to cope with new TDAQ requirements



New detectors on the Inner Barrel Part

Trigger efficiency achievable with upgraded system (blue and green) compared to legacy system in the worse case scenario (red)

More about TGC in [Kotaro's](#) and [Daisuke](#) posters

More about L0 muon trigger in [Shota's](#) poster

Tile Calorimeter

- Full replacement of readout electronics
- Readout of Full granularity at 40 MHz for trigger signal

On detector

- About 10% PMTs will be exchanged
- New mechanical structure (Mini-Drawers) to ease maintenance
- FENICs shape and amplify PMT signals (x2 gains)

Production ongoing

- Main Boards digitise signal (12b ADCs) and control FENICs

Production done

- Daughter Boards : Serialise digital data and send to off detector with 2 Kintex Ultrascale FPGA per board

Production soon to start

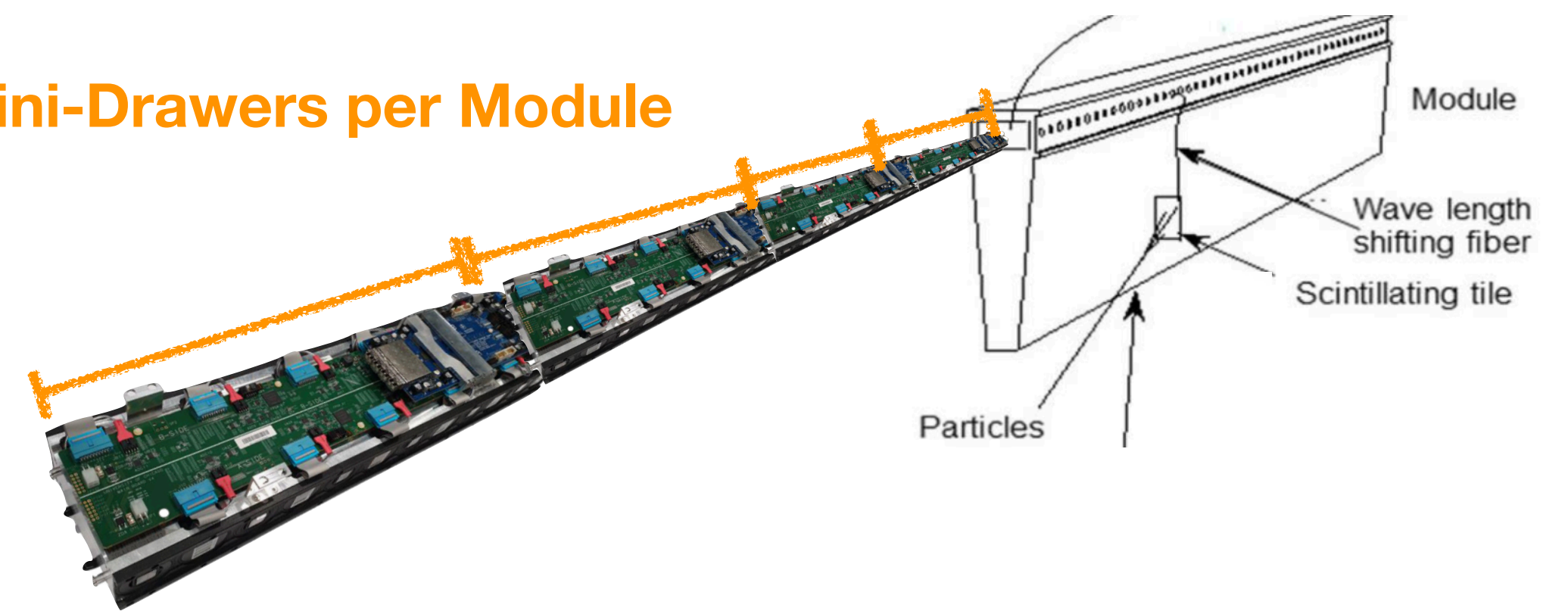
Off detector

- Pre-processor (Ppr) boards compute energy deposits, provide data to Trigger and DAQ

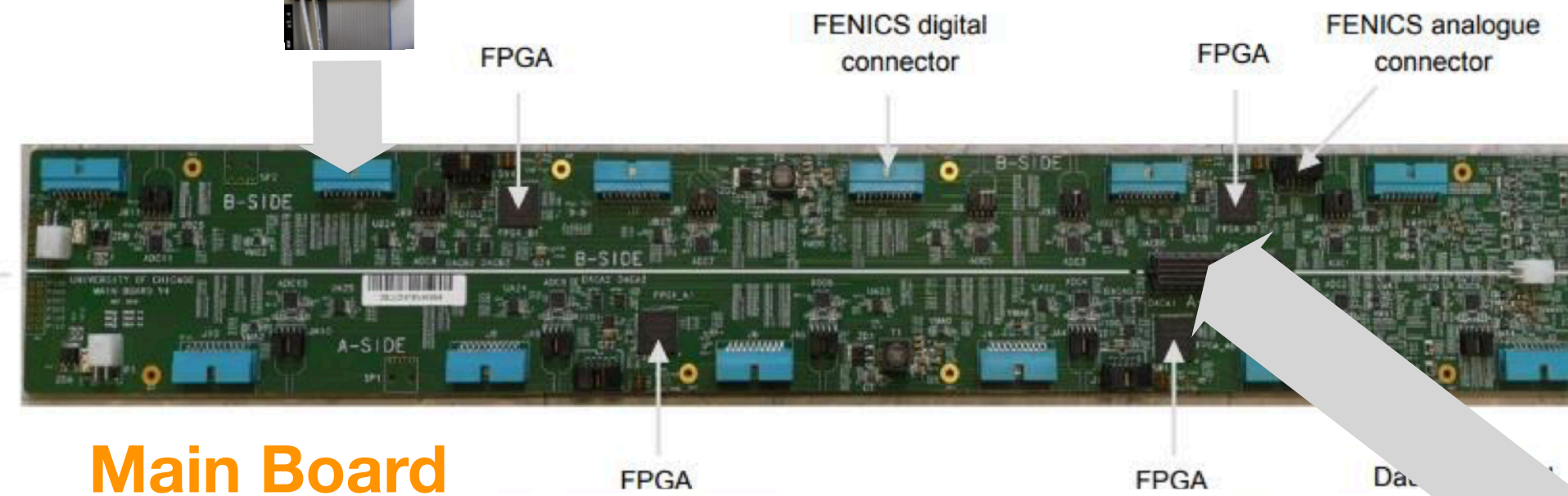
Pre-production under tests

- ATCA Carrier board
- With 4 Compact Processing Modules (KU 115 FPGA)
- Rear Module TDAQi (KU+)

4 Mini-Drawers per Module



FENICs



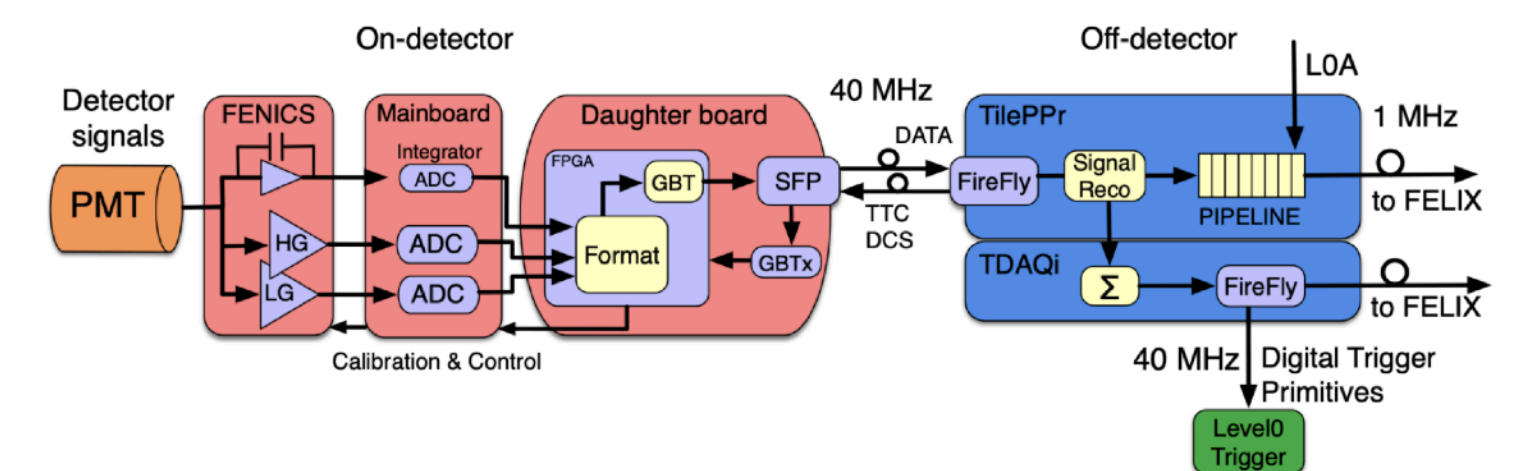
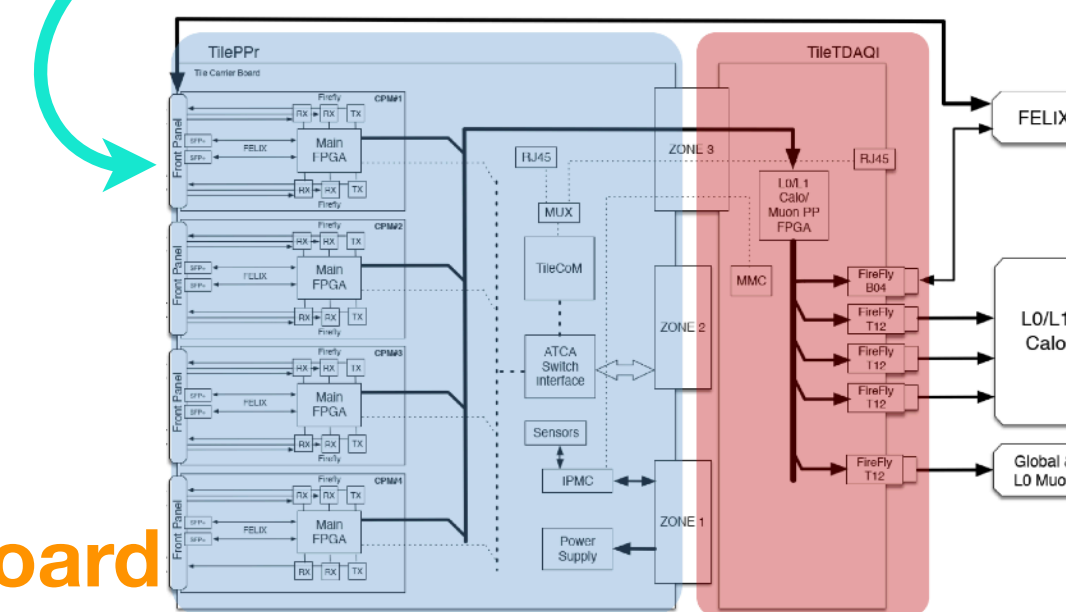
Main Board



Daughter Board v6.4

Optical fibers
32 x Trunks of 216 fibres

PPr ATCA Board

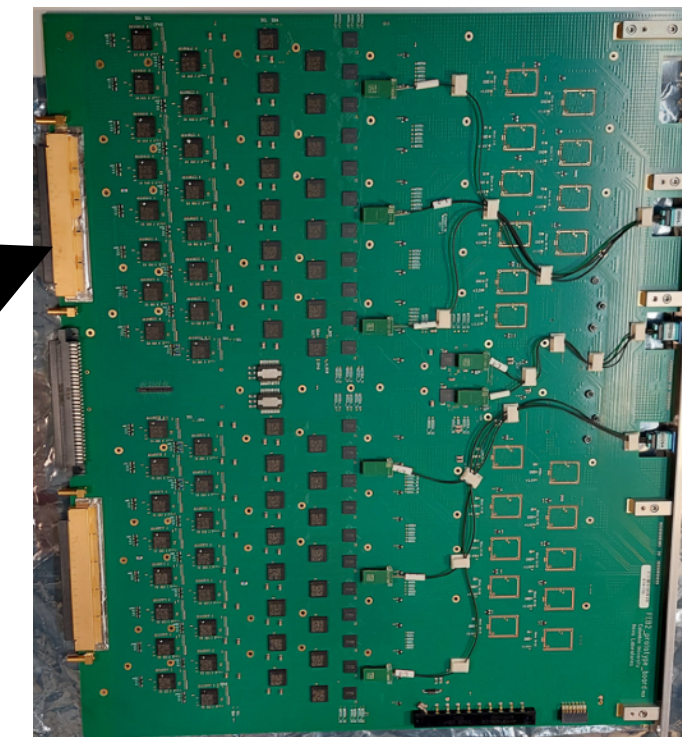


Liquid Argon Calorimeter

- Full exchange of electronics for precision readout
- 1524 Front-End boards(FEB2) send digitised data @40 MHz off-detector
Design is almost finished
⇒ Noise test still needed in fully loaded crate
- 122 Calibration boards to inject calibration pulse
Board design almost done
- 30 LATOURNETT (timing and Control)
=> High fanout board with 13 Cyclone10 FPGA in single ATCA board
Building of 2nd version of prototype board ongoing
- 278 LASP (Digital Processor)
=> Contains 2 big FPGA for Energy processing @40 MHz
Redesign of the board with new Agilex7 FPGA almost done
- Investigation ongoing about usage of Neural-Networks embedded in FPGA to process energies in high pileup environment and at 40 MHz

More details in [Jules poster](#)

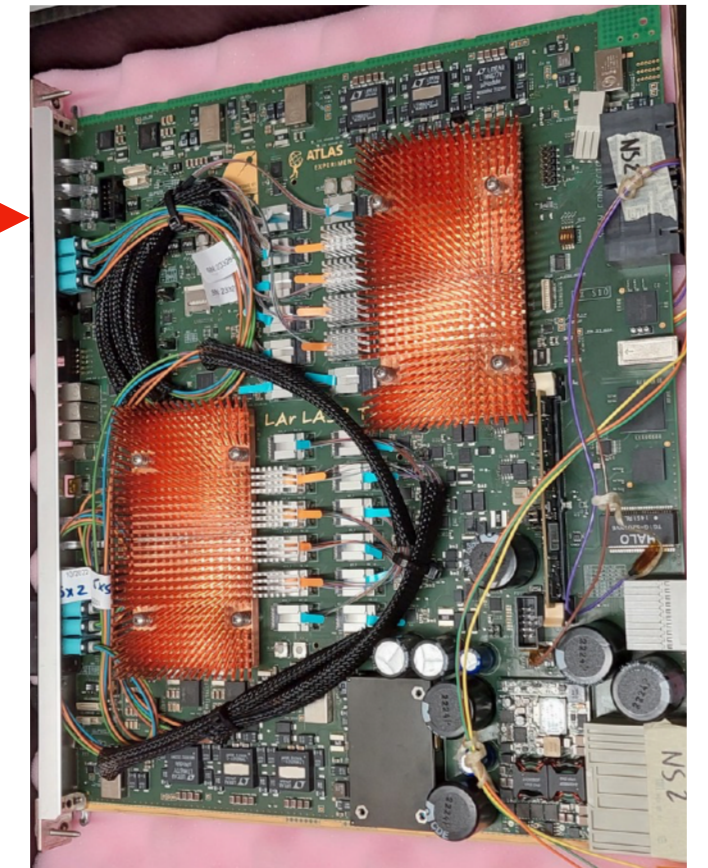
FEB2 prototype



Analog signal

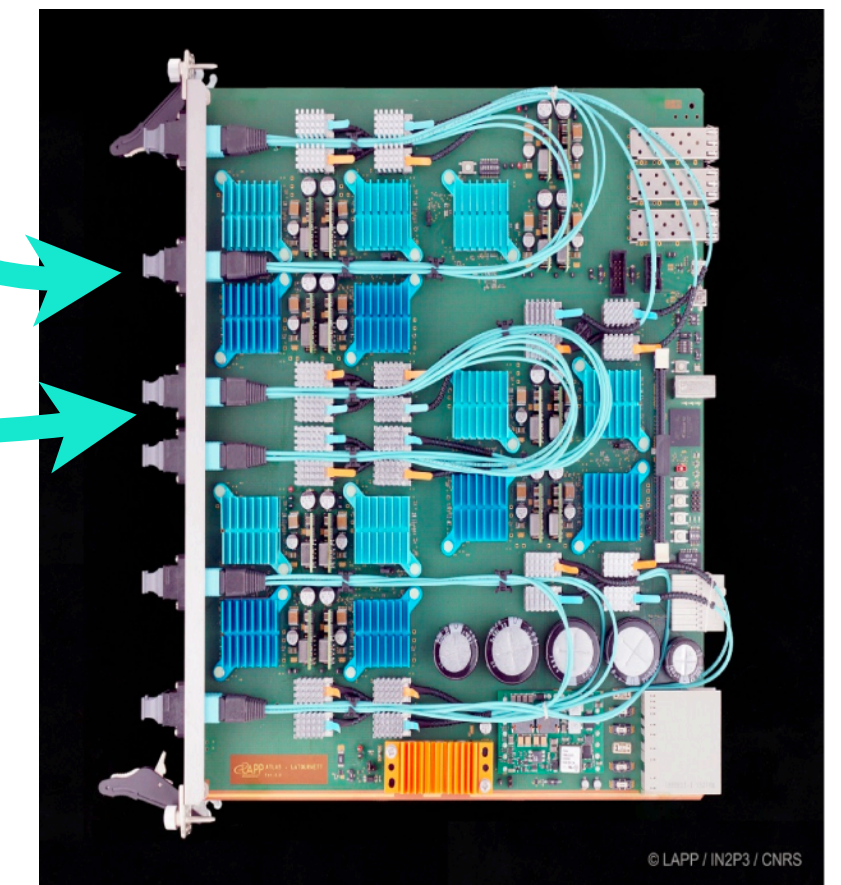
Data (Digital)

LASP test board



Control

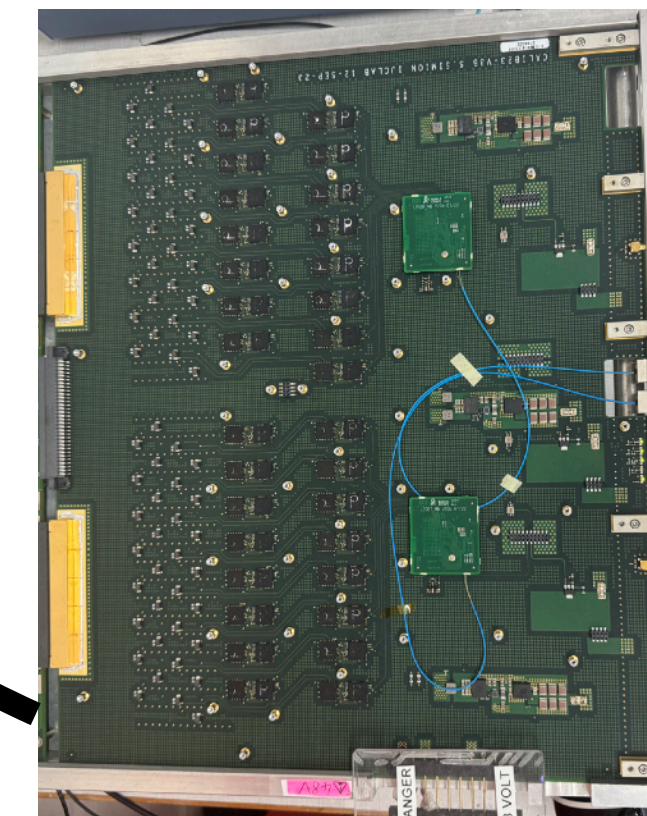
LATOURNETT v1



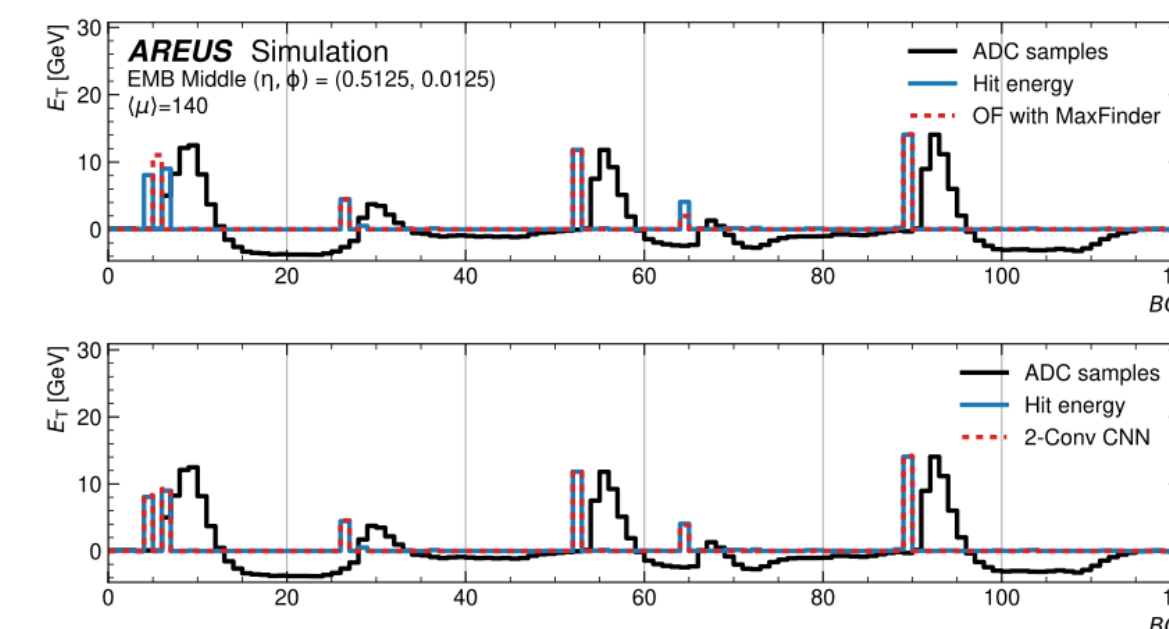
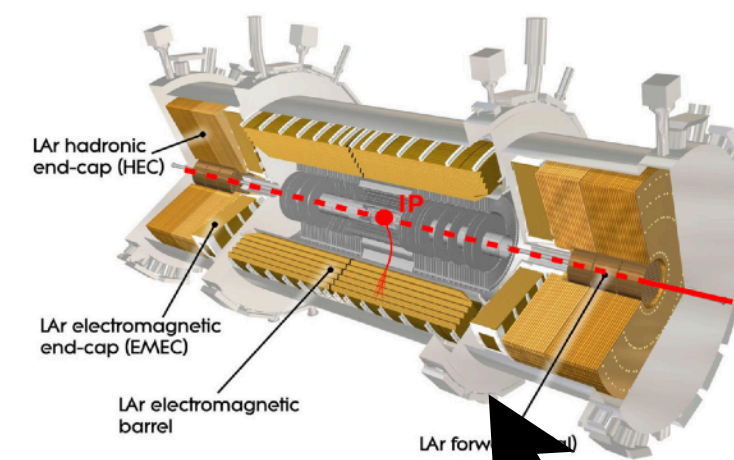
Control

More details in [Huacheng poster](#)

Calibration board prototype



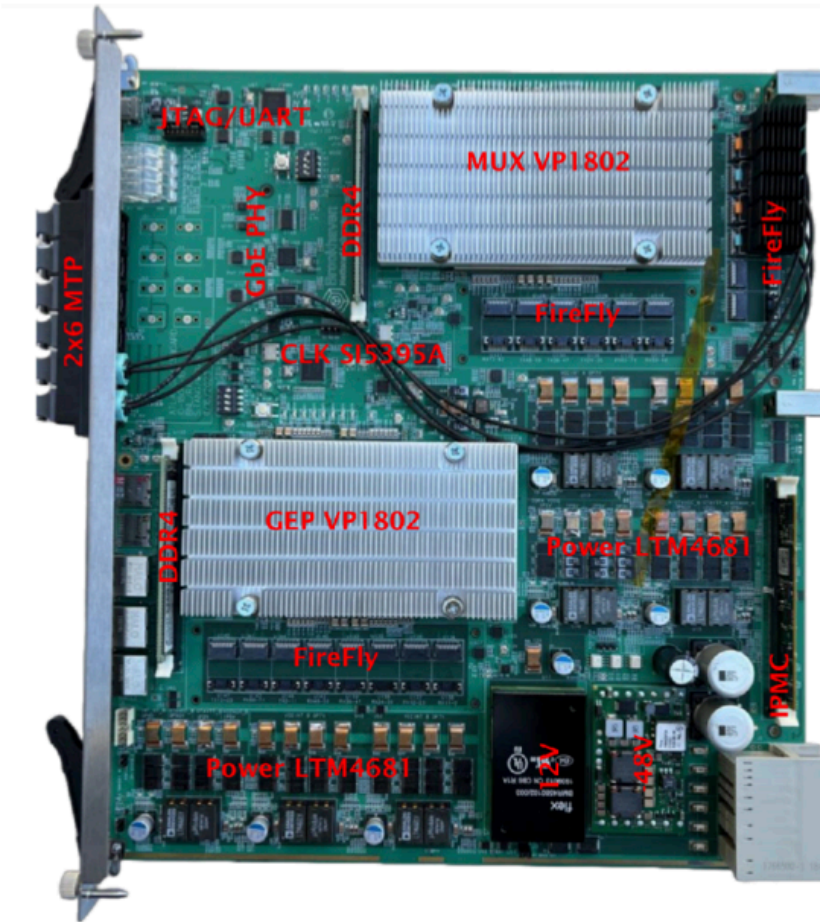
Calibration pulse



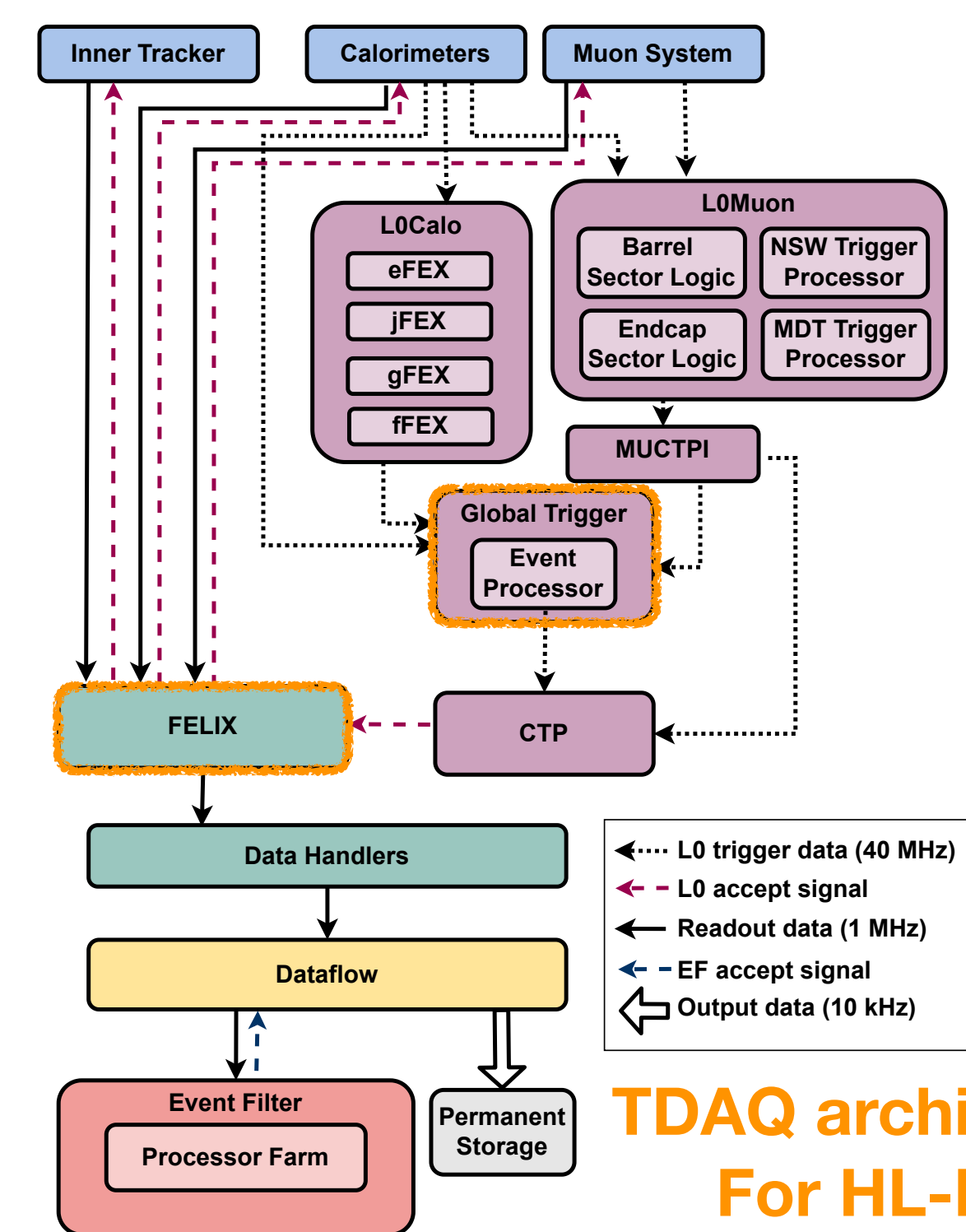
Comparison of energy reconstruction with optimal filtering and neural network

TDAQ

- Upgrade of the hardware trigger (L0) system :
 - Recording rate should reach 1 MHz (x10 compared to LHC program)
 - Trigger latency up to $10 \mu s$ (x4 compared to LHC program)
 - Global trigger aggregates event data into single FPGA VP1802
 - ⇒ Receive Trigger Object from Phase-1 electronics (FEXes + MuCTPI)
 - ⇒ Full Calorimeters granularity
 - ⇒ Object Level & Event level reconstruction
- New timing distribution system (LTI)
- Upgrade of data acquisition
 - New readout card (FELIX) with higher bandwidth and processing capabilities
 - Upgrade of Event filter farm
 - ⇒ Technology evaluation ongoing (FPGA/CPU/GPU)

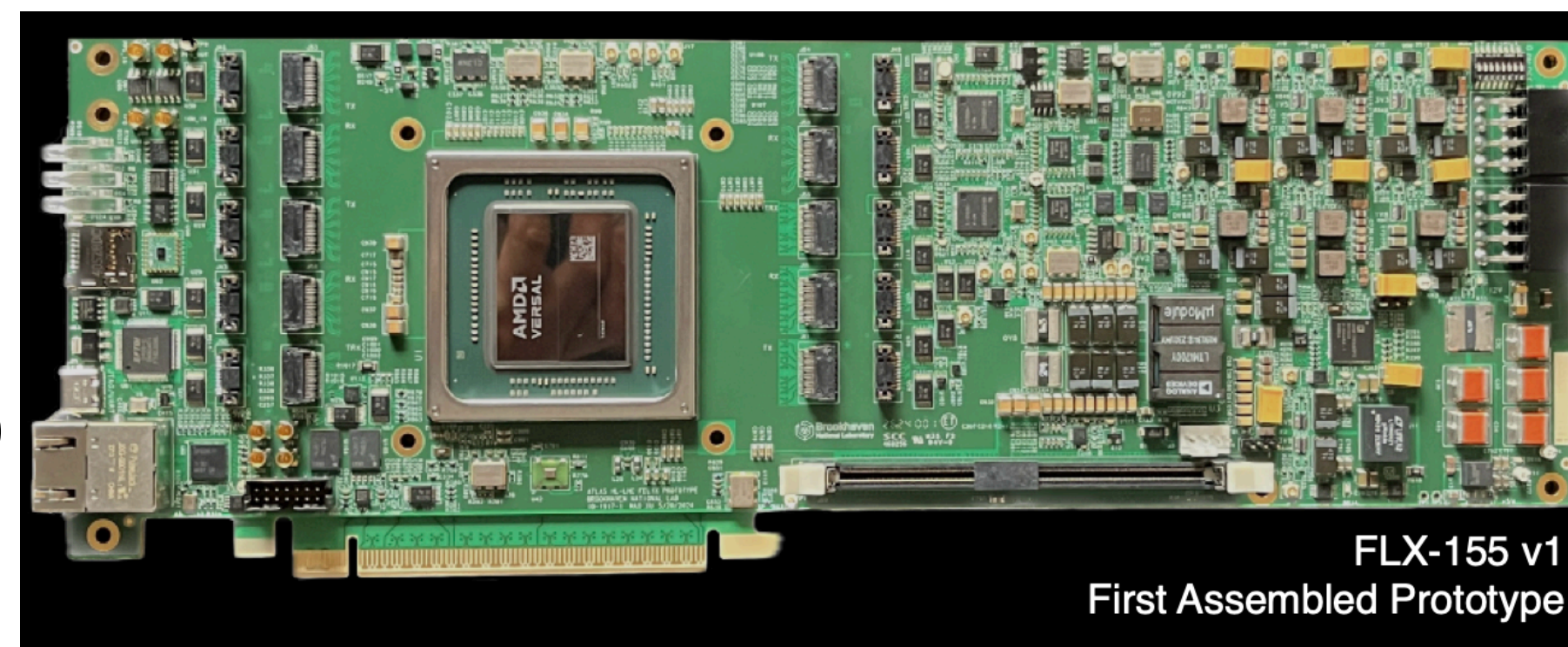


Global Trigger ATCA board

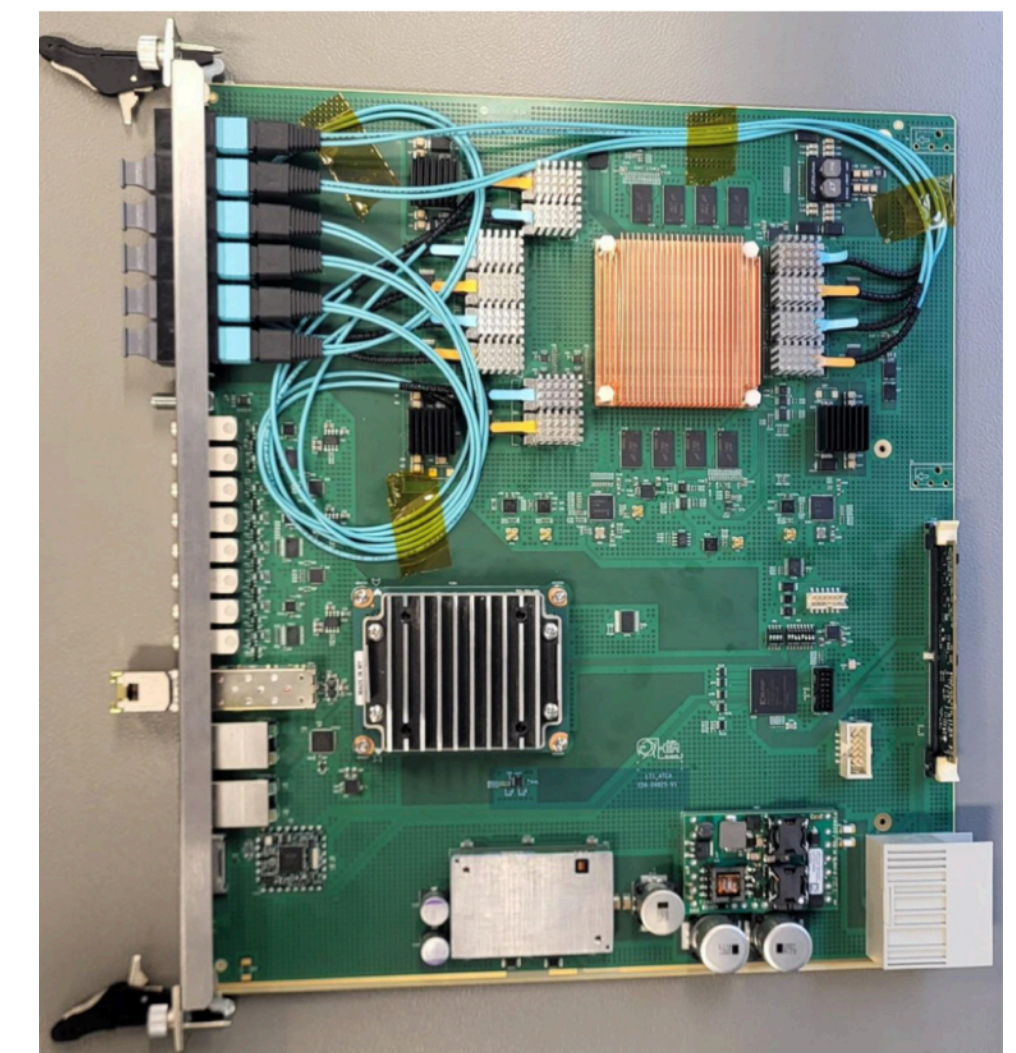


TDAQ architecture For HL-LHC

More about trigger strategies in [Theodoros' talk](#)



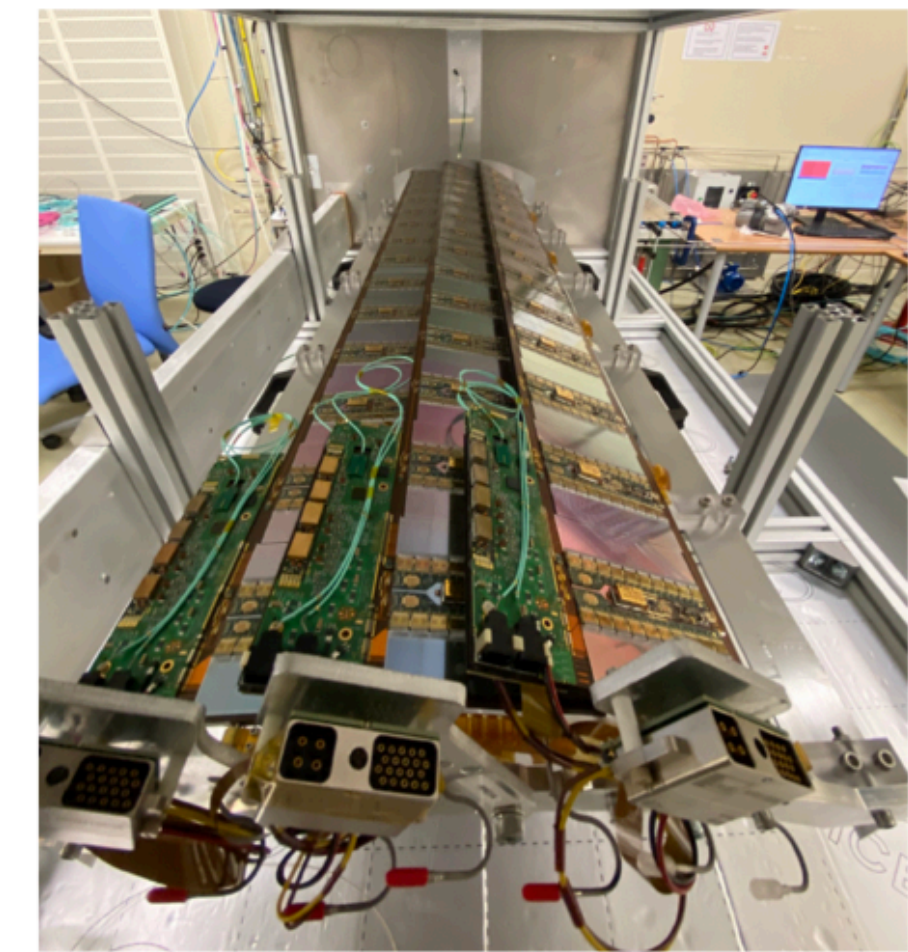
Prototype of FELIX for HL-LHC



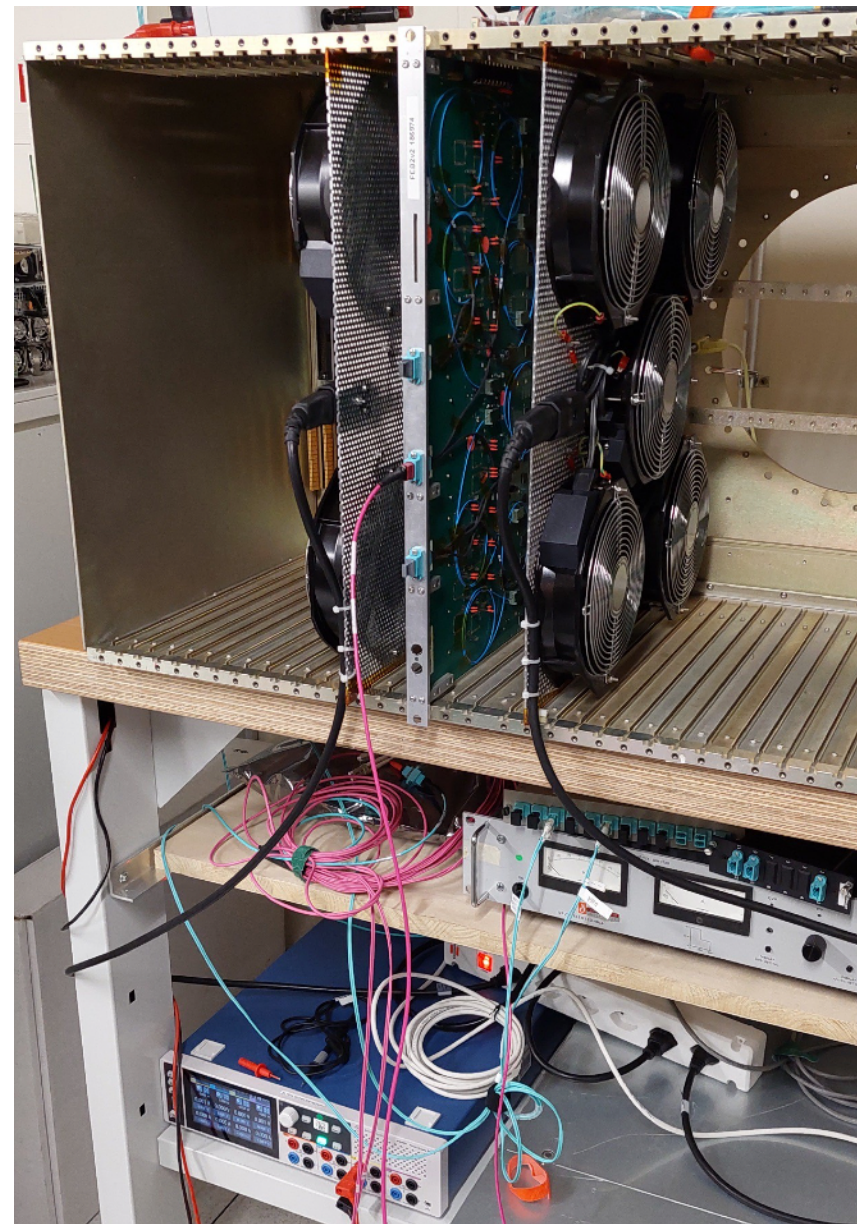
LTI Prototype

Integration

- Many efforts on all the projects to build system test to integrate their components
- Also test ongoing between TDAQ/DCS/Infrastructure and systems



Assembly of 3 ITK strips staves



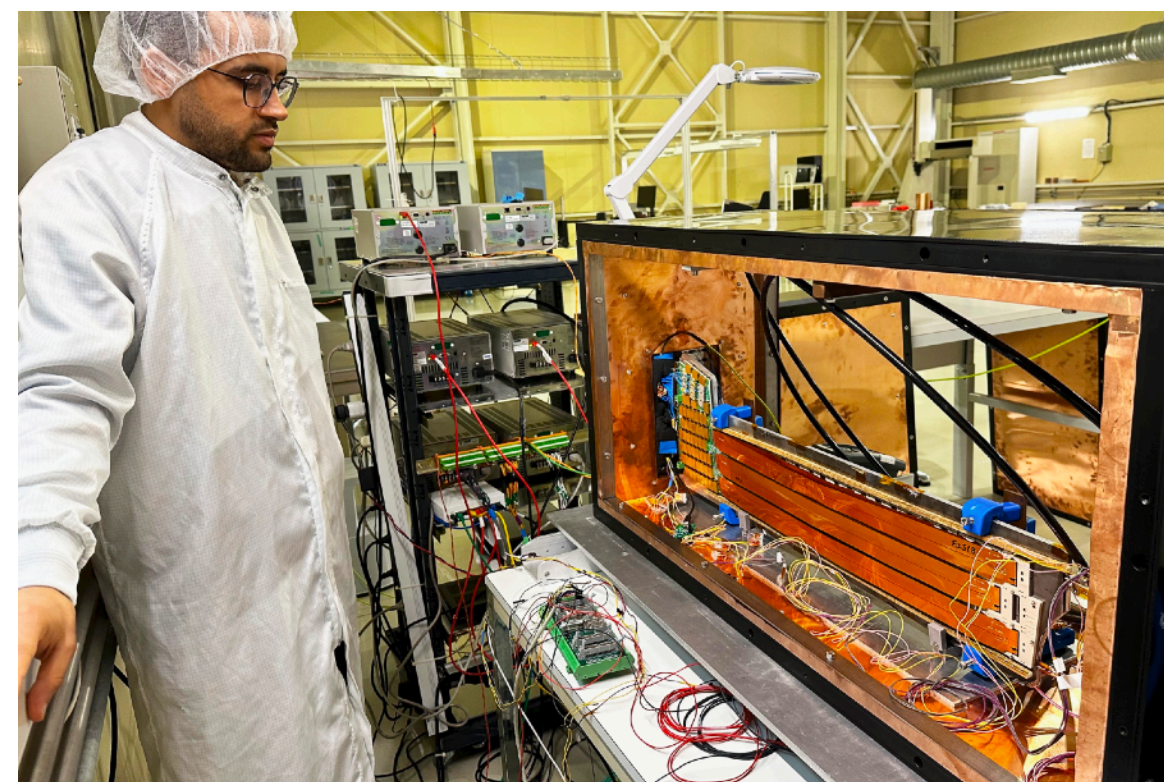
LAr FEB2 prototype
in Front End crate



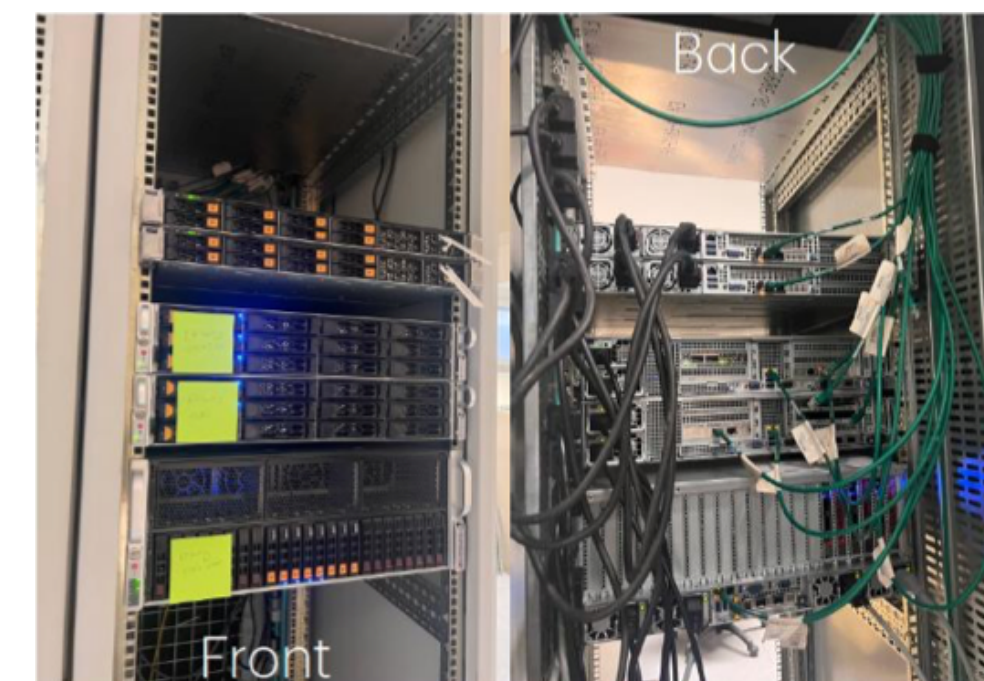
Integration between HGTD and
new timing system (LTI) board



ITK pixel
Pre-production
loaded longeron



HGTD prototype

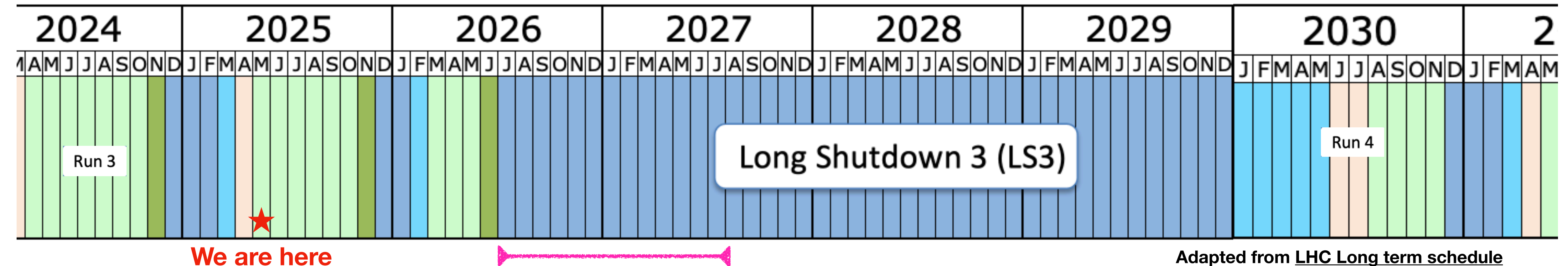


TDAQ Event Filtering Slice



Muon sMDT integration

Planning for LS3 and HL-LHC

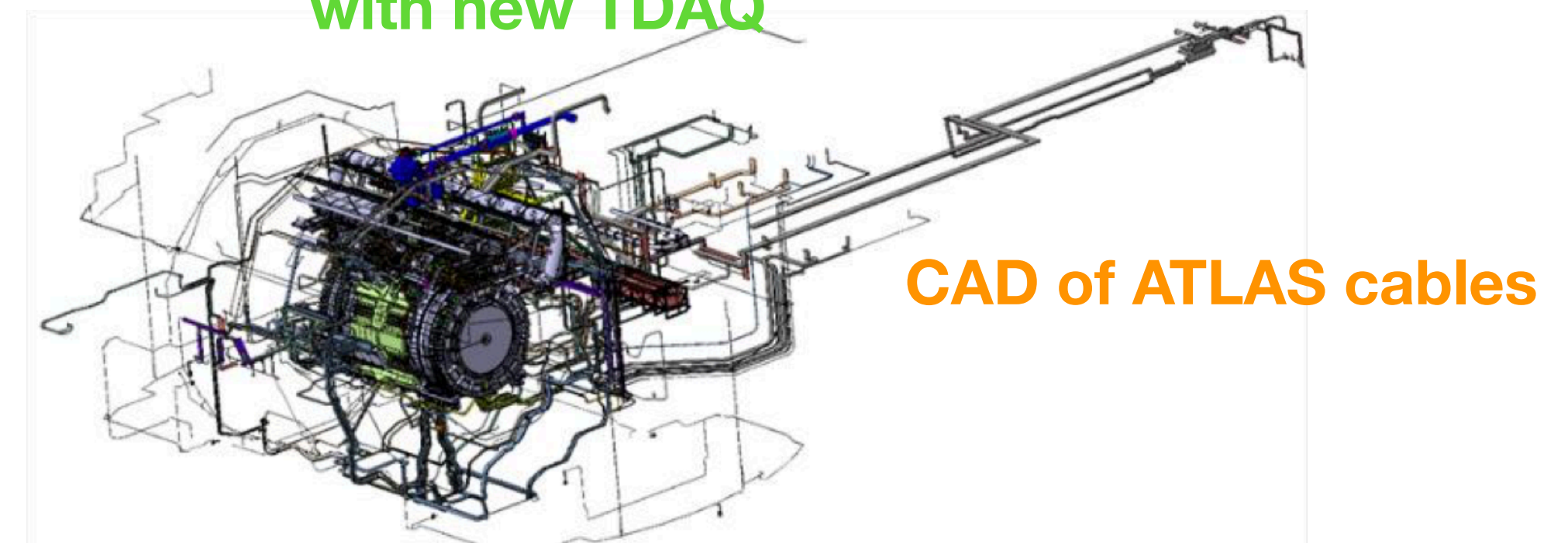


Dismantling +
Infrastructure
upgrade

Calorimeters + Muon
Upgrade

ITK + HGTD installation
Recommissioning
with new TDAQ

- Inclusion of new detector services (CO₂ bi-phase cooling station)
- Major rework of electrical infrastructure / rack room
- New cooling structure for Calorimeter/HGTD
- Up to 1000 km of cable to remove and re-install



Conclusion

- To be able to operate ATLAS during the HL-LHC a vast detector upgrade program is ongoing
- For most of the project the mass production of critical components has started
- Integration phase has started and will be critical for success of the whole upgrade project
- Many other project ongoing toward HL-LHC (new tracking reconstructions, forward detector upgrade, computing...)
- LS3 is now very close, we will soon enter an intense period of activity at Point-1, to be ready in 2030

