An ultra-energy-efficient 10GS/s Analog-to-Digital Converter for Radio Astronomy

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INTRODUCTION

- ❖ Analog to Digital Converters (ADC) are ubiquitous and critical components of the modern life, which enable us to interface to the analog world around us.
- ❖ For radio astronomy with instantaneous RF bandwidth of nearly 4 GHz and interference obscuring weak signals, it is essential to have high-speed and high-resolution non-interleaved ADCs.
- ❖ This research is focused on design and implementation of a high-speed (10GS/s) and high-resolution (7-bit) ADC integrated using a cost-effective CMOS technology

SELECTING THE ADC ARCHITECTURE

- ❖ An approximate classification of different ADC topologies is shown in Fig.1 illustrating the typical capability of each topology.
- ❖ Although there is a variety of ADC topologies [1], the existing structures cannot fulfill both the intended resolution and speed without time-interleaving.
- ❖ In this report we introduce an analog-delay pipeline ADC (ADP-ADC), which provides us with intended resolution and sampling rate.

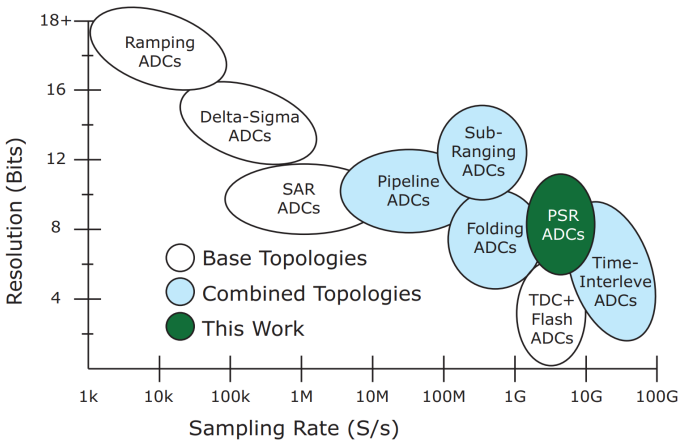


Fig.1 : ADC topology trend

ADP-ADC STRUCTURE

- ❖ Fig.2 illustrates the functional design for of such an ADP-ADC topology.
- ❖ In pipeline ADC, the signal is released before the fine ADC allowing the coarse ADC to begin capturing the next sample in parallel with the fine ADC.
- ❖ In the ADP-ADC configuration the coarse ADC can begin the next conversion cycle without waiting for any other step in the pipeline.

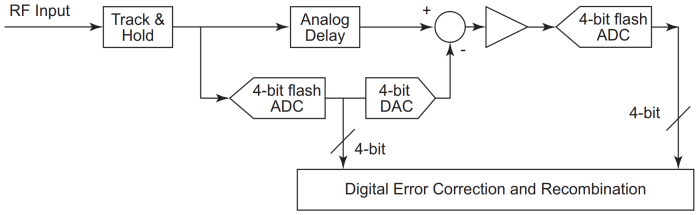


Fig.2 : Possible implementation of ADP-ADC structure

COARSE & FINE ADC

- ❖ Coarse and fine ADCs have typical flash ADC topology shown in Fig.3. For illustration only, the flash ADC input is single ended and thus has a reference ladder. The main difference between this and the comparator used in this work is that the comparators take a differential signal without the use of a reference ladder [2].

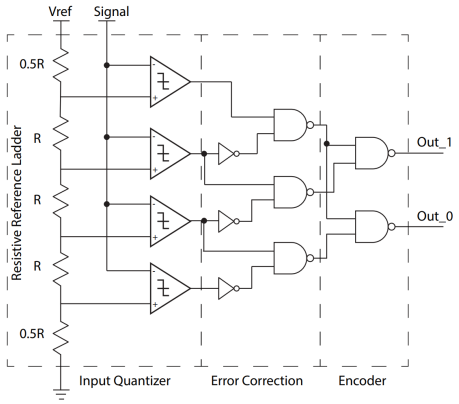
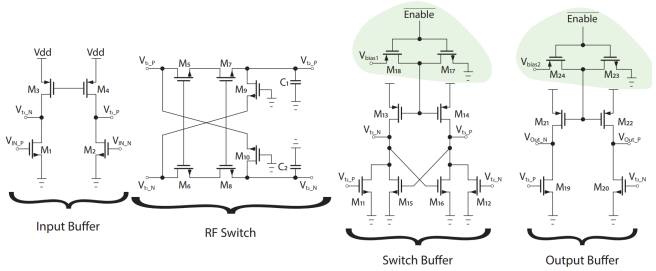


Fig.3 : Typical flash ADC architecture for single-ended inputs

TRACK & HOLD

- ❖ In any pipeline ADC design the timing between stages is critical and a way to hold the input signal is often required. The hold time allows for some flexibility between stages as the signal is passed from one stage to the next.
- ❖ The track and hold circuit (T/H) was developed in a joint effort within the MiNT research group [3].



CONCLUSION

- ❖ A new approach to combining ADCs to increase resolution was presented and allows higher sampling-speed as compared to the Sub-Ranging (SR) or pipeline ADC designs.
- ❖ The ADP-ADC topology developed in this work has higher potential to increase figure of merit (FOM).

REFERENCES

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