University of Victoria | Graduate Studies

Notice of the Final Oral Examination for the Degree of Doctor of Philosophy

of

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MSc (Military Technical College, Egypt)
BSc (Military Technical College, Egypt)

"Advanced Techniques for Improving Radar Performance"

Department of Electrical and Computer Engineering

Monday, November 18, 2019
10:30 A.M.
Engineering / Computer Science Building
Room 468

Supervisory Committee:
Dr. Panajotis Agathoklis, Department of Electrical and Computer Engineering, University of Victoria (Co-Supervisor)
Dr. Fayez Gebali, Department of Electrical and Computer Engineering, UVic (Co-Supervisor)
Dr. Sudhakar Ganti, Department of Computer Science, UVic (Outside Member)

External Examiner:
Dr. Majid Ahmadi, Department of Electrical and Computer Engineering, University Windsor

Chair of Oral Examination:
Dr. Timothy Iles, Department of Pacific and Asian Studies, UVic

Dr. David Capson, Dean, Faculty of Graduate Studies

Abstract

Wideband beamforming have been widely used in modern radar systems. One of the powerful wideband beamforming techniques that is capable of achieving a high selectivity over a wide bandwidth is the nested array (NA) beamformer. Such a beamformer consists of nested antenna arrays, 2-D spatio-temporal filters, and multirate filterbanks. Speed of operation is bounded by the speed of the hardware implementation.

This dissertation presents the use of a systematic methodology for design space exploration of the NA beamformer basic building blocks. The efficient systolic array design in terms of the highest possible clock speed of each block was selected for hardware implementation. The proposed systolic array designs and the conventional designs were implemented in FPGA hardware to verify their functionality and compare their performance. The implementations results confirm that the proposed systolic array implementations are faster and requires less hardware resources than the published designs. The overall beamformer FPGA implementation is constructed based on the analysis of efficient systolic arrays designs of the beamformer building blocks. The implemented overall structure is then validated to ensure its proper operation. Further, the implementation performance is evaluated in terms of accuracy and error analysis in comparison to the MATLAB simulations. The new methodology is based on the systematic methodology to close the gap between the modern wideband radar I/O rates and the silicon operating speed This new methodology is applied to the interpolator block as an example. The proposed methodology is simulated and tested using MATLAB object oriented programming (OOP) to ensure the proper operation.