The Department of Electrical and Computer Engineering is seeking a qualified individual to teach ECE 470 Artificial Intelligence / ECE 569A Selected Topics in Computer Engineering for the Summer 2018 (May to August) academic term. These two courses are expected to share lectures as well as some assignments and tests. Students registered in ECE 569A are required to complete a project. The calendar description of the ECE 470 and ECE 569A courses can be found below:

**ECE 470**
- Units: 1.5
- Formerly: CENG 420, CENG 490
- **Artificial Intelligence**
  - Philosophy of artificial intelligence. AI programs and languages, representations and descriptions, exploiting constraints. Rule-based and heuristic systems. Applications to engineering.
  - Note: Credit will be granted for only one of ECE 470, ECE 490 (if taken in the same topic), CENG 420, CENG 490 (if taken in the same topic), CSC 421, ELEC 490 (if taken in the same topic).
  - Prerequisite(s): Minimum fourth-year standing in the Faculty of Engineering.

**ECE 569A**
- Units: 1.5
- Formerly: ELEC 569A, ELEC 669
- **Selected Topics in Computer Engineering**
  - Notes:
    - Credit will be granted for only one of ECE 569A, ELEC 569A (if taken in the same topic), ELEC 669 (if taken in the same topic).
    - May be taken more than once for credit in different topics to a maximum of 3 units.
    - Variable content course.

**REQUIRED QUALIFICATIONS AND EXPERIENCE**
- The successful individual will have a Ph.D. and relevant industrial experience with the subject matter.
- Prior teaching experience at a university level is an asset.
- Salary is commensurate with the qualifications and follows the Sessional Lecturer Salary Grid included in the agreement between the University of Victoria and CUPE Local 4163 (Component 3).
- Professional engineering registration (PEng) is highly desired.
- **IF YOU ARE A GRADUATE STUDENT APPLYING FOR THIS POSITION, YOUR APPLICATION MUST INCLUDE A LETTER FROM YOUR SUPERVISOR(S) INDICATING HIS/HER/THEIR AGREEMENT WITH YOU ACCEPTING THIS POSITION SHOULD IT BE OFFERED TO YOU.**

The availability of this position is subject to funding and enrollment criteria. The University of Victoria reserves the right to fill additional teaching assignments from the pool of applicants for this posting.

The University of Victoria is an equity employer and encourages applications from women, persons with disabilities, visible minorities, and aboriginal persons.

**TO APPLY:** Please submit an expression of interest together with a recent CV via email to [eceasst@uvic.ca](mailto:eceasst@uvic.ca)
- Attention: Chair, Department of Electrical and Computer Engineering by: **16 February 2018**.

The anticipated date by which employment decisions will be made is **23 February 2018.**