Faculty of Engineering
COURSE OUTLINE

ELEC 330 – Electronic Circuits: I
Spring 2017 CRN: 21145/21146

Instructor:
Dr. H.L. Kwok
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Office Hours:
Days: W
Time: 15:30-17:00
Location: EOW425

Course Objectives
This course deals with the principle of operation and design issues related to modern electronic circuits. The advancement of electronic circuits has been primarily due to the invention of new devices and design techniques and it is desirable for practicing engineers to have an updated perspective and understanding on state-of-the-art electronic circuits and future trends.

Learning Outcomes
LO-1: Study the properties and operation of active devices

  SLO-1.1: Students learn of the properties of nonlinear junction devices such as the junction diodes and the transistors

LO-2: Study the generation of simple waveforms

  SLO-2.1: Students learn how nonlinear device properties are utilized and exploited in circuit design especially for integrated circuits

  SLO-2.2: Student learn how meaningful waveforms can be generated in circuits and their functionalities in the context of circuit design

LO-3: Study signal amplification and transistor circuits

  SLO-3.1: Students learn how signal amplification can be facilitated including performance optimization with respect to gain, input and output impedance matching and bandwidth issues

  SLO-3.2: Students learn various forms of biasing in amplifier circuits

LO-4: Study the multi-stage circuits and their design

  SLO-4.1: Students learn how multi-stage circuits are coupled and related interface design compromises

LO-4: Study device models and simulations
SLO-4.1: Students learn device modeling and circuit simulations

LO-5: Study logic gates and simple sequential circuits

SLO-5.1: Students learn logic gates, switching and sequential circuits and their functionality

**Syllabus**
Nonlinear devices; modeling and application of diodes; rectifiers, voltage regulators; waveform shaping circuits (chapter 2)

Biasing of bipolar and field-effect transistors (Chapters 5 and 8)

Small-signal amplifiers and multistage amplifiers (Chapters 6 and 9)

Nonlinear applications of transistors including: digital circuits such as inverters, (logic) gates and flip-flops (Chapters 4 and 9)

Circuit design; simulations; implementation; and testing (Lab manual)

**Lectures:**
A-Section(s): A01/A02 CRN 21145/21146
Days: TWF
Time: 11:30-12:20 Details available in webpage
Location: ELL167
First day of class: Jan 4
Reading Break: **Feb.13-17**
Last day of class: April 4

**Required Text:**
Title: Electronic Devices conventional current version, 9th Ed.
Author: T.L. Floyd
Publisher: Prentice Hall
Year: 2012

**Labs:**
B-Section(s) Days Time
Location: ELW

**Location:** To be posted on webpage

**Assessment:**
- Assignments: 10%
- Labs: 15%
- Mid-terms: 20% (x2) Dates: Feb. 10 (Fri) and Mar 10 (Fri)
- Final: 35%

**Optional Text:**
Course Pack for ELEC330
Author: Adam Zielinski
Available at University Bookstore

**Note:** Failure to complete all laboratory requirements will result in a grade of N being awarded for the course.
Due dates for assignments:

To be decided (normally 1 week after the assignments are given)

The final grade obtained from the above marking scheme for the purpose of GPA calculation will be based on the percentage-to-grade point conversion table as listed in the current Undergraduate Calendar.

There will be no supplemental examination for this course.

Note to Students:

Students who have issues with the conduct of the course should discuss them with the instructor first. If these discussions do not resolve the issue, then students should feel free to contact the Chair of the Department by email or the Chair's Secretary to set up an appointment.

Accommodation of Religious Observance
http://web.uvic.ca/calendar2017-01/general/policies.html

Policy on Inclusivity and Diversity
http://web.uvic.ca/calendar2017-01/general/policies.html

Standards of Professional Behaviour

You are advised to read the Faculty of Engineering document Standards for Professional Behaviour, which contains important information regarding conduct in courses, labs, and in the general use of facilities.
http://www.uvic.ca/engineering/assets/docs/professional-behaviour.pdf

Cheating, plagiarism and other forms of academic fraud are taken very seriously by both the University and the Department. You should consult the entry in the current Undergraduate Calendar for the UVic policy on academic integrity.
http://web.uvic.ca/calendar2017-01/undergrad/info/regulations/academic-integrity.html

Equality: This course aims to provide equal opportunities and access for all students to enjoy the benefits and privileges of the class and its curriculum and to meet the syllabus requirements. Reasonable and appropriate accommodation will be made available to students with documented disabilities (physical, mental, learning) in order to give them the opportunity to successfully meet the essential requirements of the course. The accommodation will not alter academic standards or learning outcomes, although the student may be allowed to demonstrate knowledge and skills in a different way. It is not necessary for you to reveal your disability and/or confidential medical information to the course instructor. If you believe that you may require accommodation, the course instructor can provide you with information about confidential resources on campus that can assist you in arranging for appropriate accommodation. Alternatively, you may want to contact the Resource Centre for Students with a Disability located in the Campus Services Building. The University of Victoria is committed to promoting, providing, and protecting a positive, and supportive and safe learning and working environment for all its members.
Course Lecture Notes

Unless otherwise noted, all course materials supplied to students in this course have been prepared by the instructor and are intended for use in this course only. These materials are NOT to be re-circulated digitally, whether by email or by uploading or copying to websites, or to others not enrolled in this course. Violation of this policy may in some cases constitute a breach of academic integrity as defined in the UVic Calendar.